EE 330
Lecture 22

- Comparison of BJT and MOS Area
- Amplifiers
- Small Signal Analysis
- Small Signal Modelling

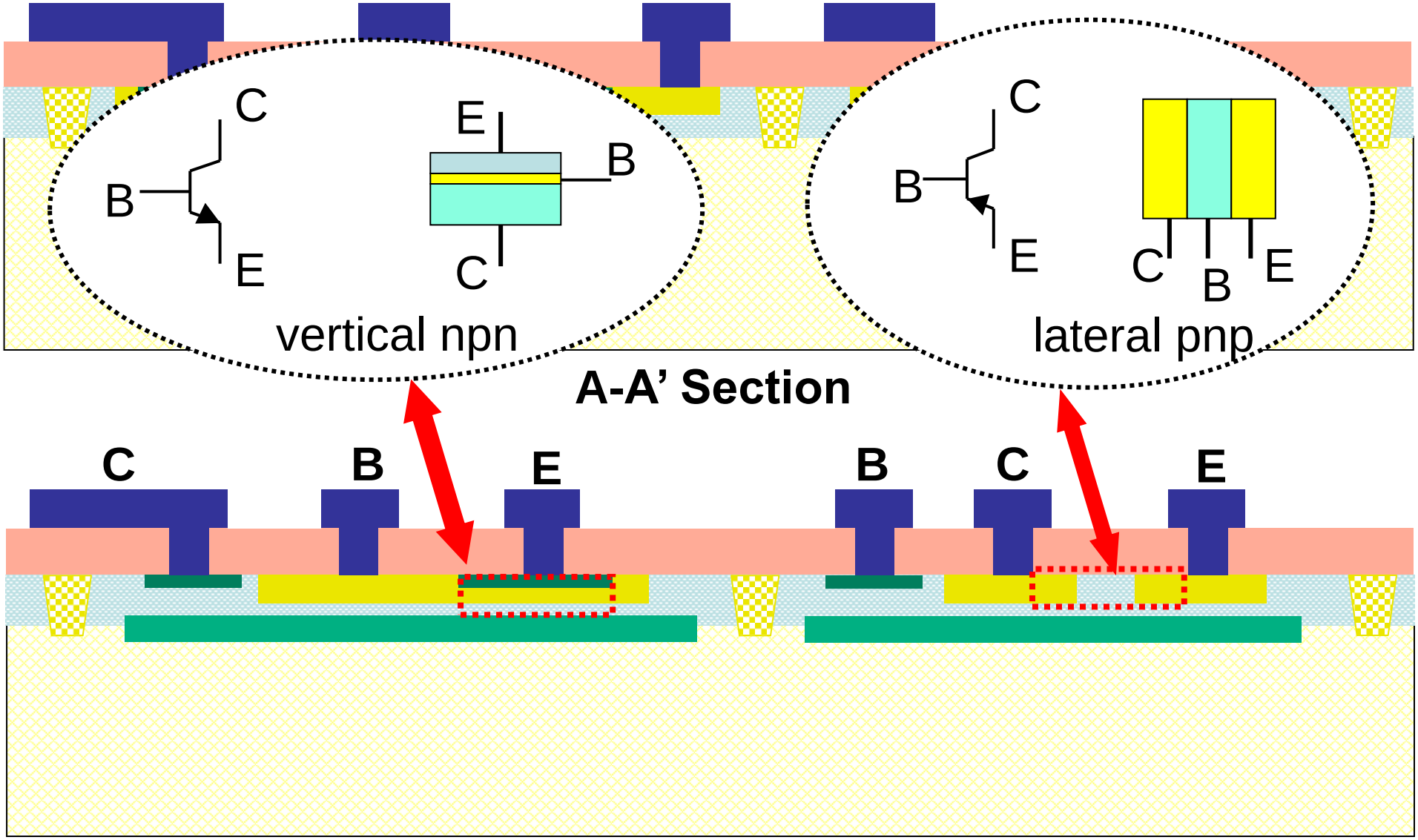
Exam Schedule

Exam 1	Friday Sept 24
Exam 2	Friday Oct 22
Exam 3	Friday Nov 19
Final	Tues Dec 14 12:00 p.m.

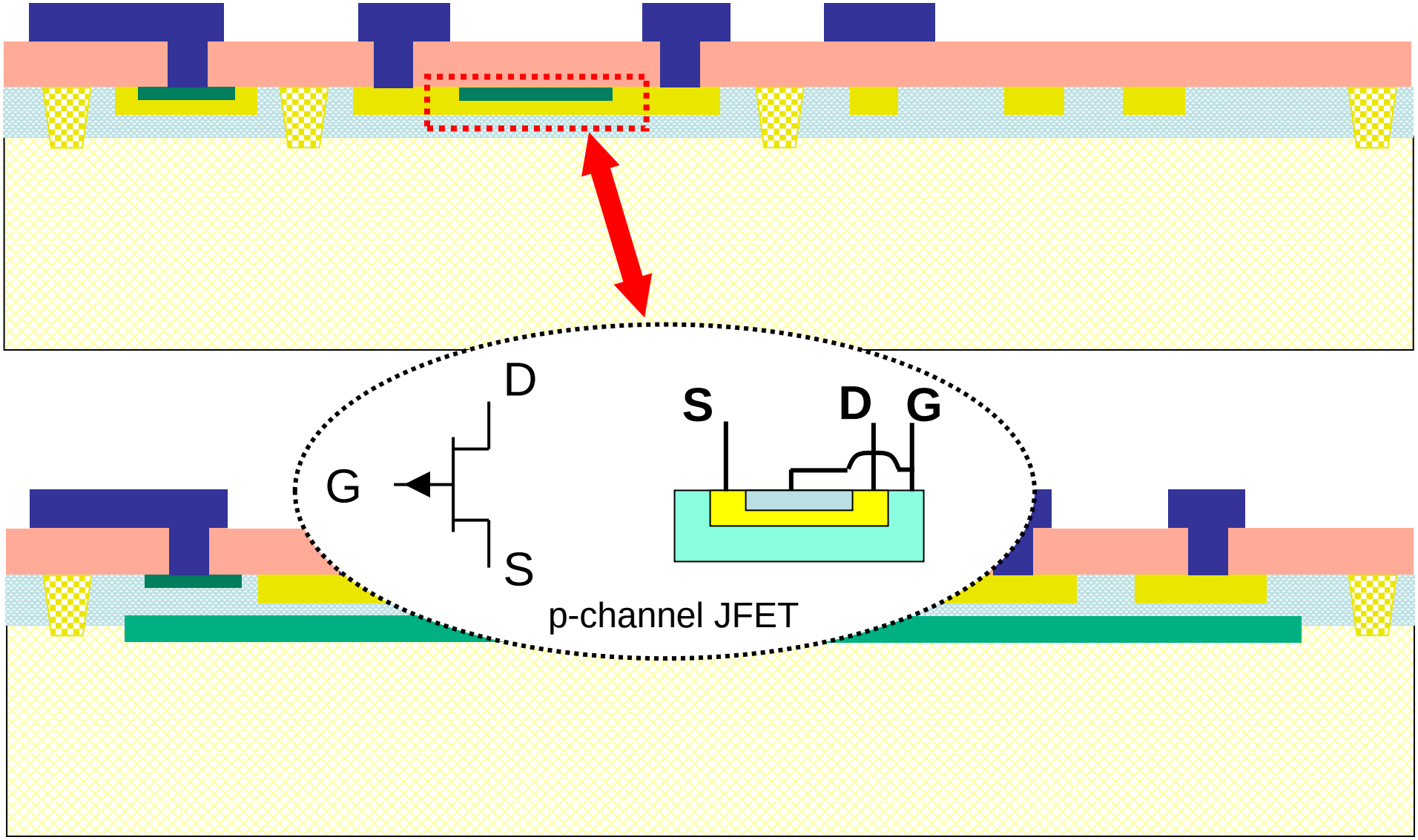
As a courtesy to fellow classmates, TAs, and the instructor

Wearing of masks during lectures and in the laboratories for this course would be appreciated irrespective of vaccination status

Review from Last Lecture

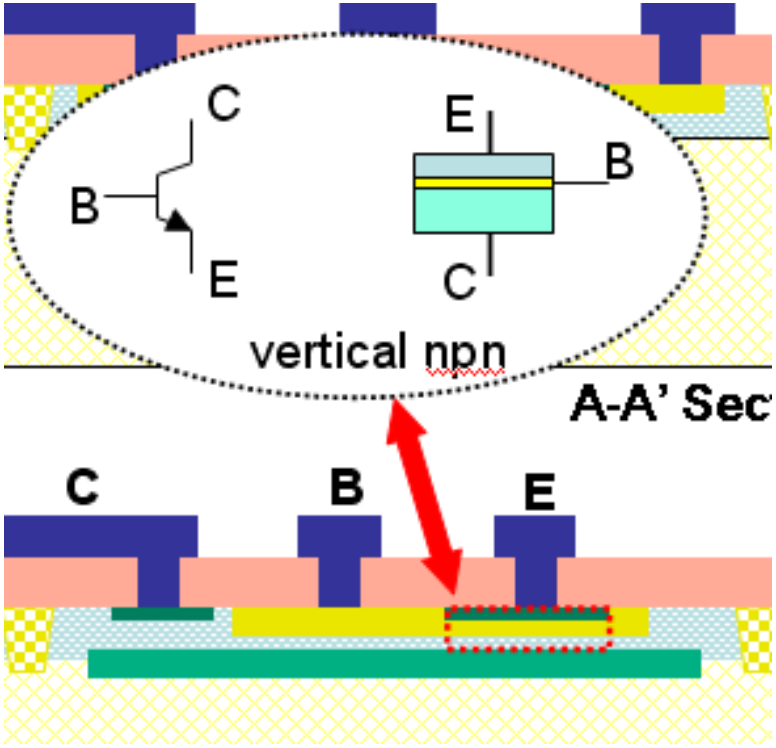


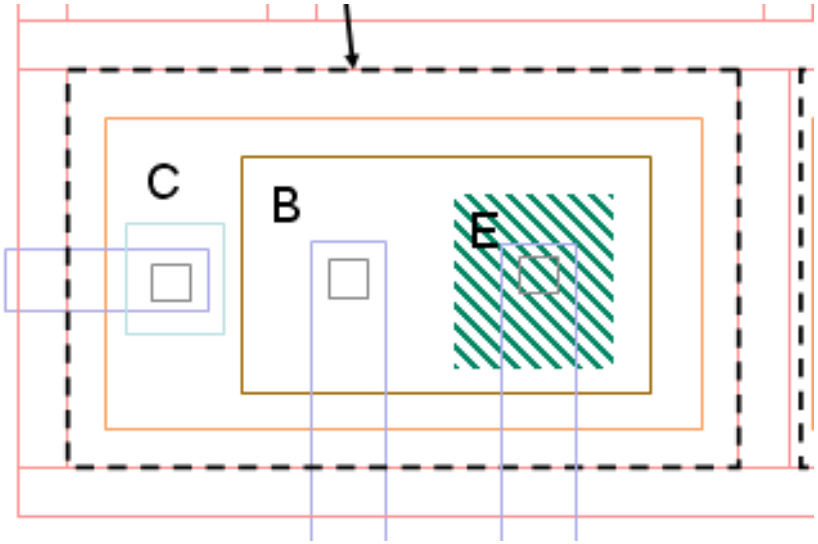
Review from Last Lecture



B-B' Section

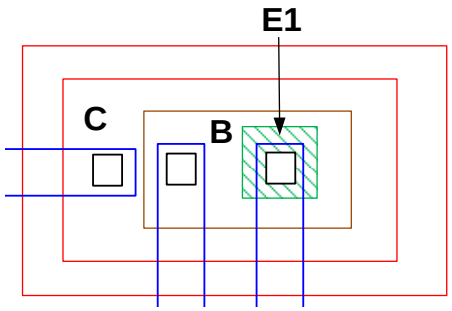
The vertical npn transistor

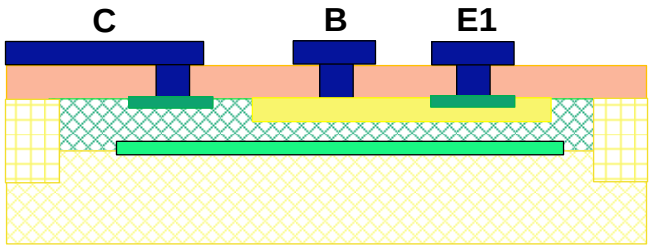


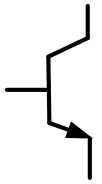


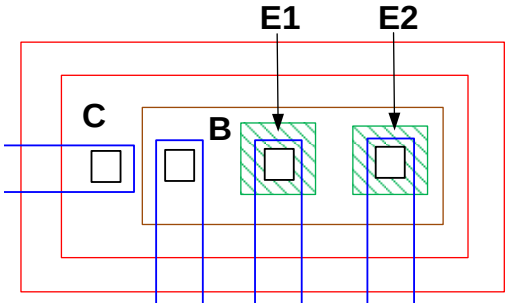
- Emitter area only geometric parameter that appears in basic device model !
- B and C areas large to get top contact to these regions
- Transistor much larger than emitter
- Multiple-emitter devices often used (TTL Logic) and don't significantly increase area
- Multiple B and C contacts often used (and multiple E contacts as well if A_E large)

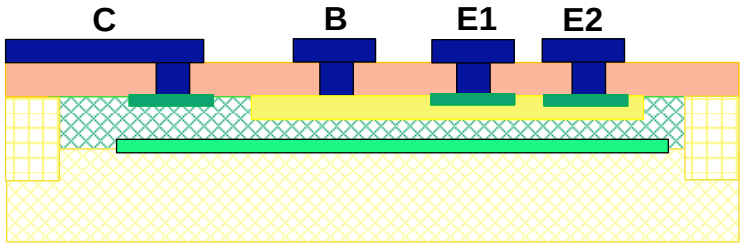
The vertical npn transistor

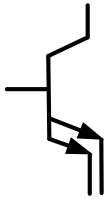












Single-emitter and Double-Emitter Transistor

Base and Collector are shared

Quirks in modeling the BJT

[a] Parameters are defined in Chapters 3 and 4.

[b] Some of these Gummel-Poon parameters differ considerably from those given in Table 2C.4. They have been obtained from curve fitting and should give good results with computer simulations. The parameters of Table 2C.4 should be used for hand analysis.

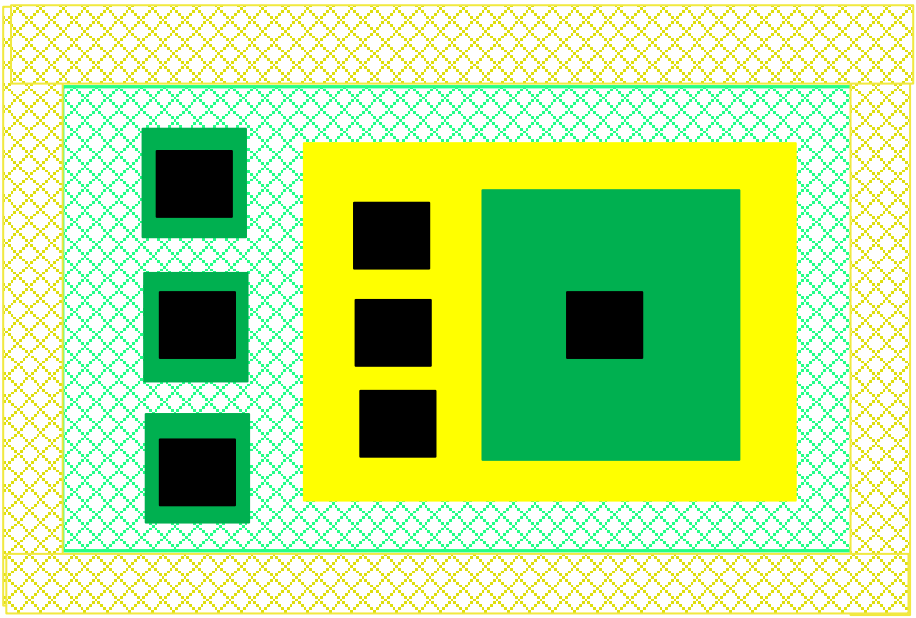
[c] Parameters that are strongly area-dependent are based upon an npn emitter area of 390 μ^2 and perimeter of 80 μ, a base area of 2200 μ^2 and perimeter of 200 μ, and a collector area of 10,500 μ^2 and perimeter of 425 μ. The lateral pnp has rectangular collectors and emitters spaced 10 μ apart with areas of 230 μ^2 and perimeters of 60 μ. The base area of the pnp is 7400 μ^2 and the base perimeter is 345 μ.

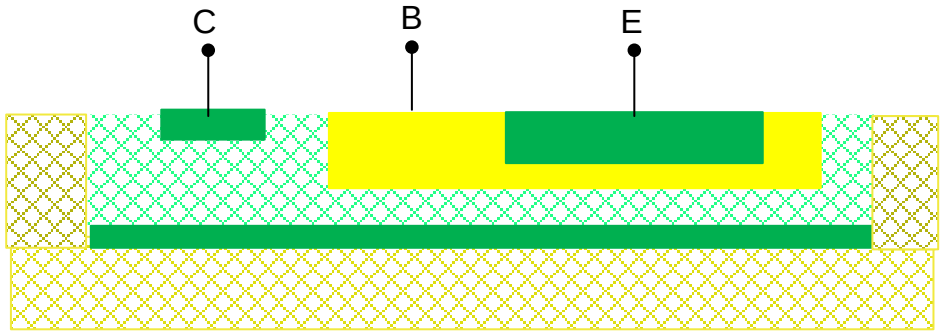
[d] CJS is set to zero for the lateral transistor because it is essentially nonexistent. The parasitic capacitance from base to substrate, which totals 1.0 pF for this device, must be added externally to the BJT.

- In contrast to the MOSFET where process parameters are independent of geometry, the bipolar transistor model is for a specific transistor !
- Area emitter factor is used to model other devices
- Often multiple specific device models are given and these devices are used directly
- Often designer can not arbitrarily set A_E but rather must use parallel combinations of specific devices and layouts

A challenge in modeling the BJT

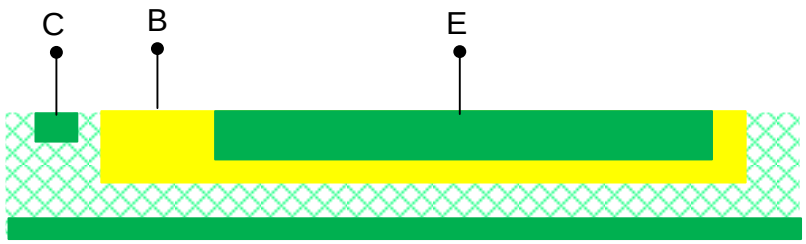
Top View of Vertical npn

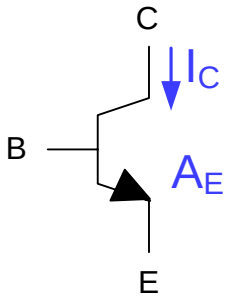




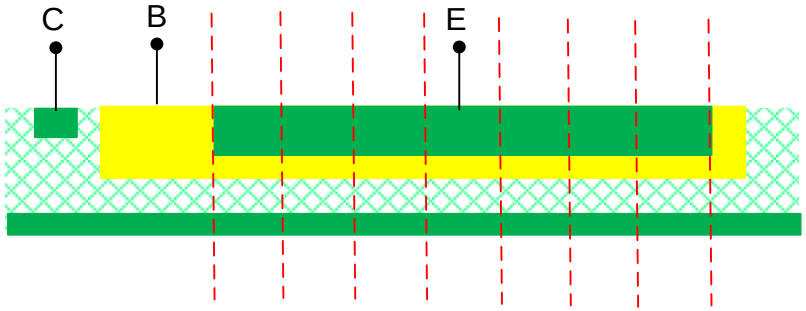
Cross-Sectional View

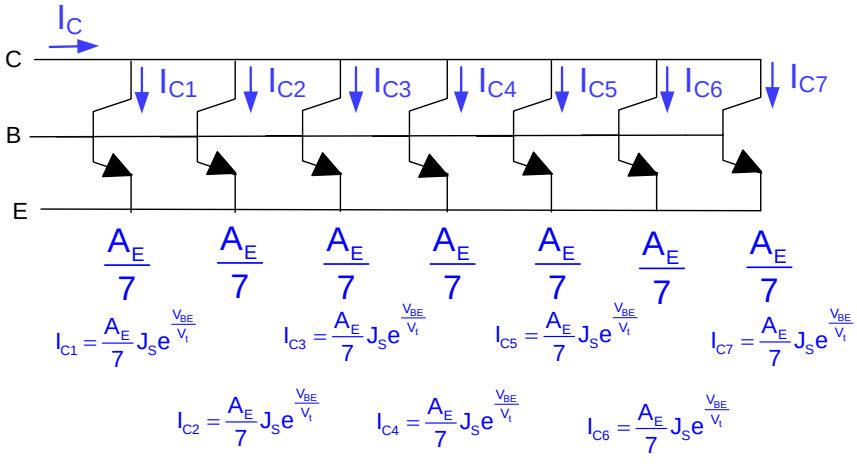
A challenge in modeling the BJT





$$I_C = A_E J_S e^{\frac{V_{BE}}{V_t}}$$

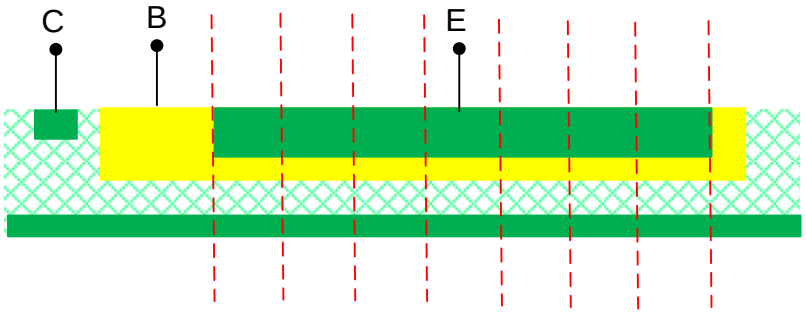


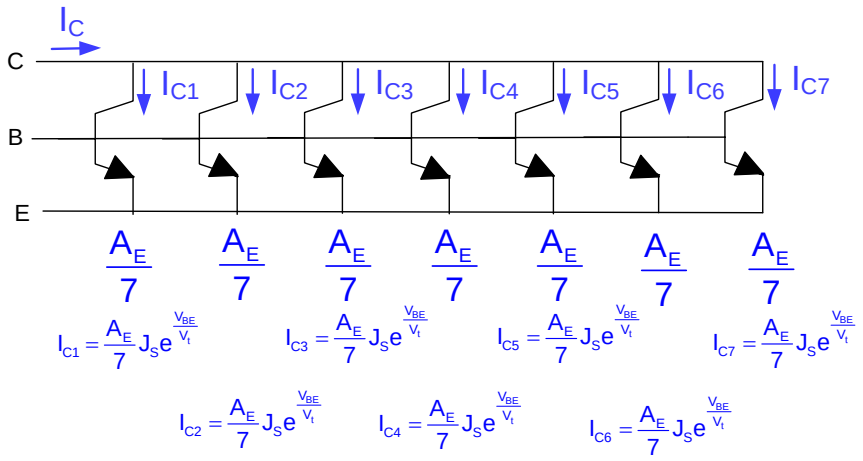


$$I_C = \sum_{i=1}^{7} \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}} = A_E J_S e^{\frac{V_{BE}}{V_t}}$$

This looks consistent but …

A challenge in modeling the BJT

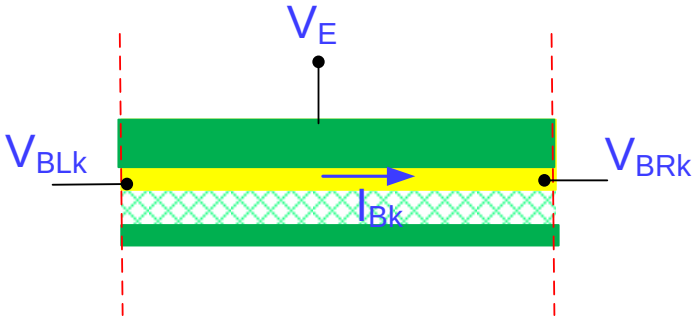




$$I_C = \sum_{i=1}^{7} \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}} = A_E J_S e^{\frac{V_{BE}}{V_t}}$$

This looks consistent but …

consider an individual slice

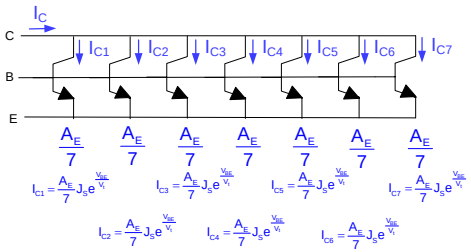


Lateral flow of base current causes a drop in base voltage across the base region

$$V_{BRk} \neq V_{BLk} \qquad I_{Ck} = \frac{A_E}{7} J_S e^{\frac{V_{BEk}}{V_t}}$$

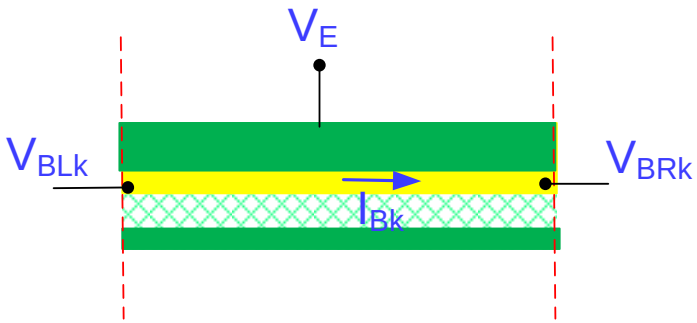
What is V_{BEk}?

A challenge in modeling the BJT



$$I_C = \sum_{i=1}^{7} \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}} = A_E J_S e^{\frac{V_{BE}}{V_t}}$$

This looks consistent but …



- Lateral flow of base current causes a drop in base voltage across the base region
- And that drop differs from one slice to the next
- So V_{BE} is not fixed across the slices
- Since current is exponentially related to V_{BE}, affects can be significant
- Termed **base spreading resistance** problem
- Strongly dependent upon layout and contact placement
- No good models to include this effect
- Major reason designer does not have control of transistor layout detail in some bipolar processes
- Similar issue does not exist in MOSFET because the corresponding gate voltage does not change with position since I_G=0

A challenge in modeling the BJT

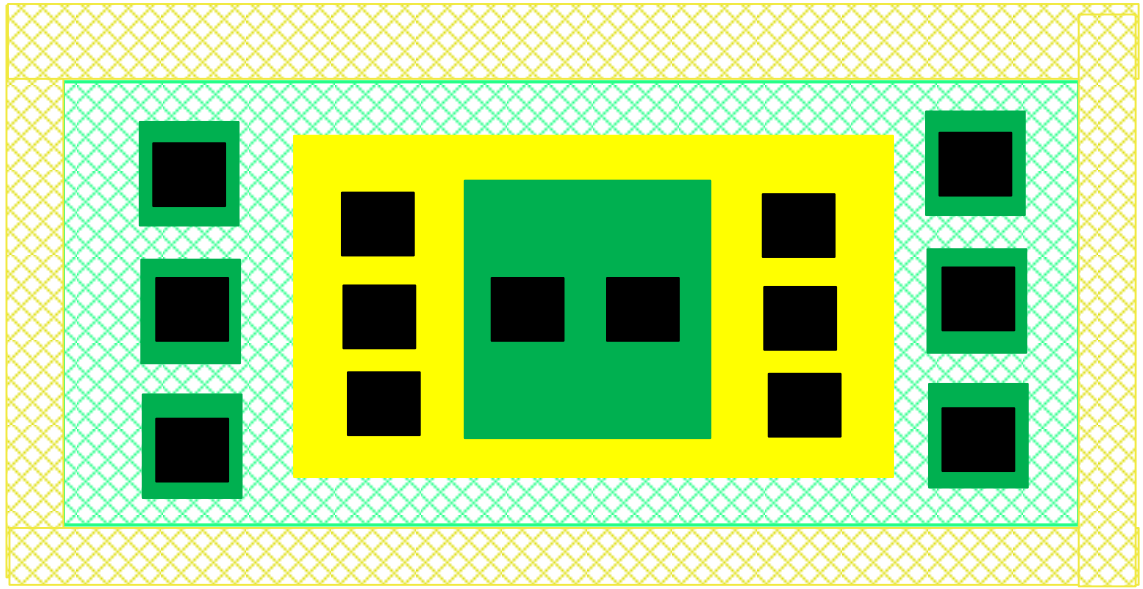
Top View of Vertical npn

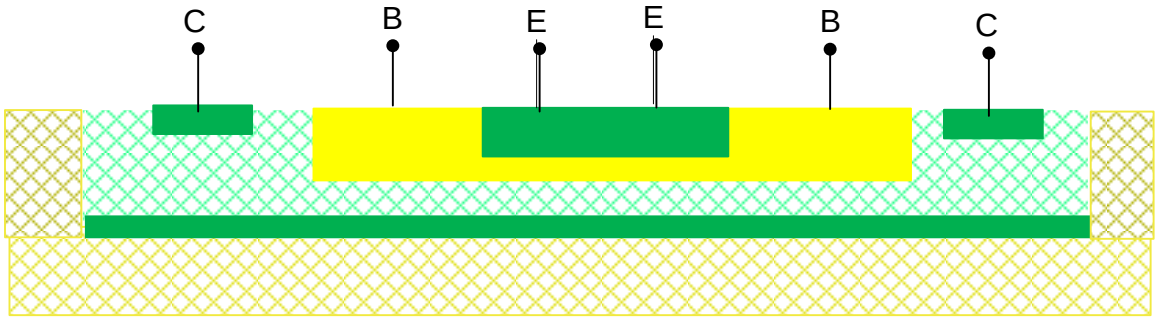
Cross-Sectional View

A challenge in modeling the BJT

What can be done about this problem ?

Top View of Vertical npn



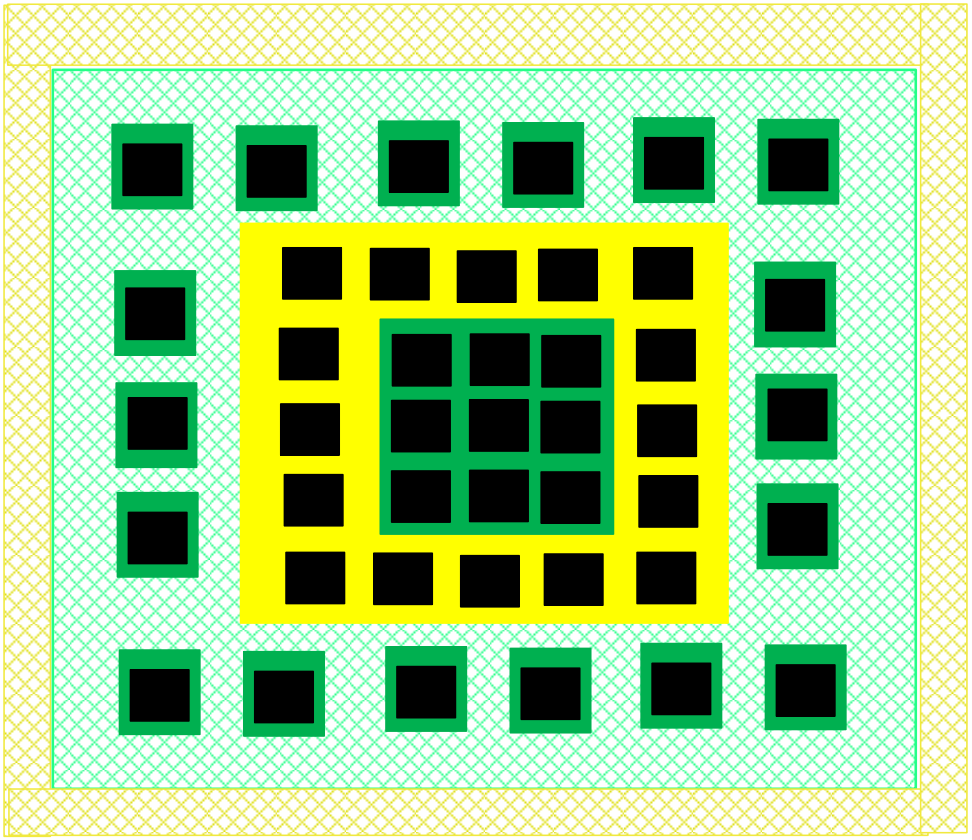


Cross-Sectional View

A challenge in modeling the BJT

What can be done about this problem ?

Top View of Vertical npn



- Often double rows of contacts used
- Area overhead can be significant
- Effects can be reduced but current flow paths are irregular

MOS and Bipolar Area Comparisions

How does the area required to realize a MOSFET compare to that required to realize a BJT?

Will consider a minimum-sized device in both processes

TABLE 2C.2
Design rules for a typical bipolar process ($\lambda = 2.5\ \mu$)
(See Table 2C.3 in color plates for graphical interpretation)

		Dimension
1.	n^+ buried collector diffusion (Yellow, Mask #1)	
	1.1 Width	3λ
	1.2 Overlap of p-base diffusion (for vertical npn)	2λ
	1.3 Overlap of n^+ emitter diffusion (for collector contact of vertical npn)	2λ
	1.4 Overlap of p-base diffusion (for collector and emitter of lateral pnp)	2λ
	1.5 Overlap of n^+ emitter diffusion (for base contact of lateral pnp)	2λ
2.	Isolation diffusion (Orange, Mask #2)	
	2.1 Width	4λ
	2.2 Spacing	24λ
	2.3 Distance to n^+ buried collector	14λ
3.	p-base diffusion (Brown, Mask #3)	
	3.1 Width	3λ
	3.2 Spacing	5λ
	3.3 Distance to isolation diffusion	14λ
	3.4 Width (resistor)	3λ
	3.5 Spacing (as resistor)	3λ
4.	n^+ emitter diffusion (Green, Mask #4)	
	4.1 Width	3λ
	4.2 Spacing	3λ
	4.3 p-base diffusion overlap of n^+ emitter diffusion (emitter in base)	2λ
	4.4 Spacing to isolation diffusion (for collector contact)	12λ
	4.5 Spacing to p-base diffusion (for base contact of lateral pnp)	6λ
	4.6 Spacing to p-base diffusion (for collector contact of vertical npn)	6λ

5. Contact (Black, Mask #5)	
5.1 Size (exactly)	$4\lambda \times 4\lambda$
5.2 Spacing	2λ
5.3 Metal overlap of contact	λ
5.4 n^+ emitter diffusion overlap of contact	2λ
5.5 p-base diffusion overlap of contact	2λ
5.6 p-base to n^+ emitter	3λ
5.7 Spacing to isolation diffusion	4λ
6. Metalization (Blue, Mask #6)	
6.1 Width	2λ
6.2 Spacing	2λ
6.3 Bonding pad size	$100\ \mu \times 100\ \mu$
6.4 Probe pad size	$75\ \mu \times 75\ \mu$
6.5 Bonding pad separation	$50\ \mu$
6.6 Bonding to probe pad	$30\ \mu$
6.7 Probe pad separation	$30\ \mu$
6.8 Pad to circuitry	$40\ \mu$
6.9 Maximum current density	$0.8\ \text{mA}/\mu$ width
7. Passivation (Purple, Mask #7)	
7.1 Minimum bonding pad opening	$90\ \mu \times 90\ \mu$
7.2 Minimum probe pad opening	$65\ \mu \times 65\ \mu$

Consider Initially the Emitter in the BJT surrounded by a base region

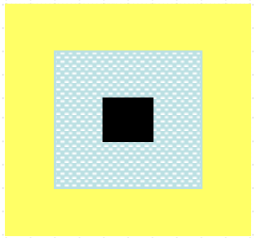


TABLE 2C.2
Design rules for a typical bipolar process ($\lambda = 2.5\ \mu$)
(See Table 2C.3 in color plates for graphical interpretation)

		Dimension
1.	n^+ buried collector diffusion (Yellow, Mask #1)	
	1.1 Width	3λ
	1.2 Overlap of p-base diffusion (for vertical npn)	2λ
	1.3 Overlap of n^+ emitter diffusion (for collector contact of vertical npn)	2λ
	1.4 Overlap of p-base diffusion (for collector and emitter of lateral pnp)	2λ
	1.5 Overlap of n^+ emitter diffusion (for base contact of lateral pnp)	2λ
2.	Isolation diffusion (Orange, Mask #2)	
	2.1 Width	4λ
	2.2 Spacing	24λ
	2.3 Distance to n^+ buried collector	14λ
3.	p-base diffusion (Brown, Mask #3)	
	3.1 Width	3λ
	3.2 Spacing	5λ
	3.3 Distance to isolation diffusion	14λ
	3.4 Width (resistor)	3λ
	3.5 Spacing (as resistor)	3λ
4.	n^+ emitter diffusion (Green, Mask #4)	
	4.1 Width	3λ
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	4.3 p-base diffusion overlap of n^+ emitter diffusion (emitter in base)	2λ
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5. Contact (Black, Mask #5)	
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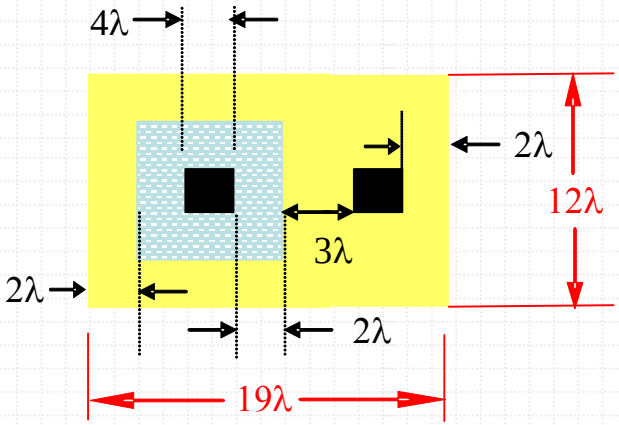
5.5 p-base diffusion overlap of contact	2λ
5.6 p-base to n^+ emitter	3λ
5.7 Spacing to isolation diffusion	4λ
6. Metalization (Blue, Mask #6)	
6.1 Width	2λ
6.2 Spacing	2λ
6.3 Bonding pad size	$100\ \mu \times 100\ \mu$
6.4 Probe pad size	$75\ \mu \times 75\ \mu$
6.5 Bonding pad separation	$50\ \mu$
6.6 Bonding to probe pad	$30\ \mu$
6.7 Probe pad separation	$30\ \mu$
6.8 Pad to circuitry	$40\ \mu$
6.9 Maximum current density	0.8 mA/μ width
7. Passivation (Purple, Mask #7)	
7.1 Minimum bonding pad opening	$90\ \mu \times 90\ \mu$
7.2 Minimum probe pad opening	$65\ \mu \times 65\ \mu$

From design rules (left to right) 4.3, 5.1, 5.4, 5.6, 5.5



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2. Isolation diffusion (Orange, Mask #2)	
2.1 Width	4λ
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2.3 Distance to n^+ buried collector	14λ
3. p-base diffusion (Brown, Mask #3)	
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3.2 Spacing	5λ
3.3 Distance to isolation diffusion	14λ
3.4 Width (resistor)	3λ
3.5 Spacing (as resistor)	3λ
4. n^+ emitter diffusion (Green, Mask #4)	
4.1 Width	3λ
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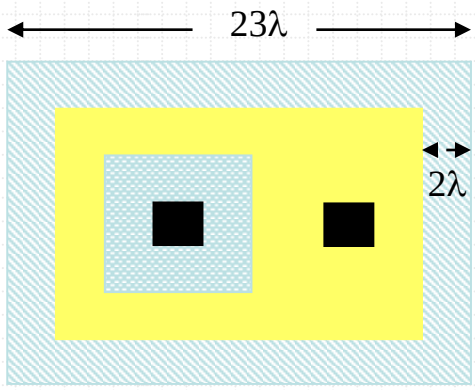
4.3 p-base diffusion overlap of n^+ emitter diffusion (emitter in base)	2λ
4.4 Spacing to isolation diffusion (for collector contact)	12λ
4.5 Spacing to p-base diffusion (for base contact of lateral pnp)	6λ
4.6 Spacing to p-base diffusion (for collector contact of vertical npn)	6λ

Add n+ buried for collector

From design rule 1.2



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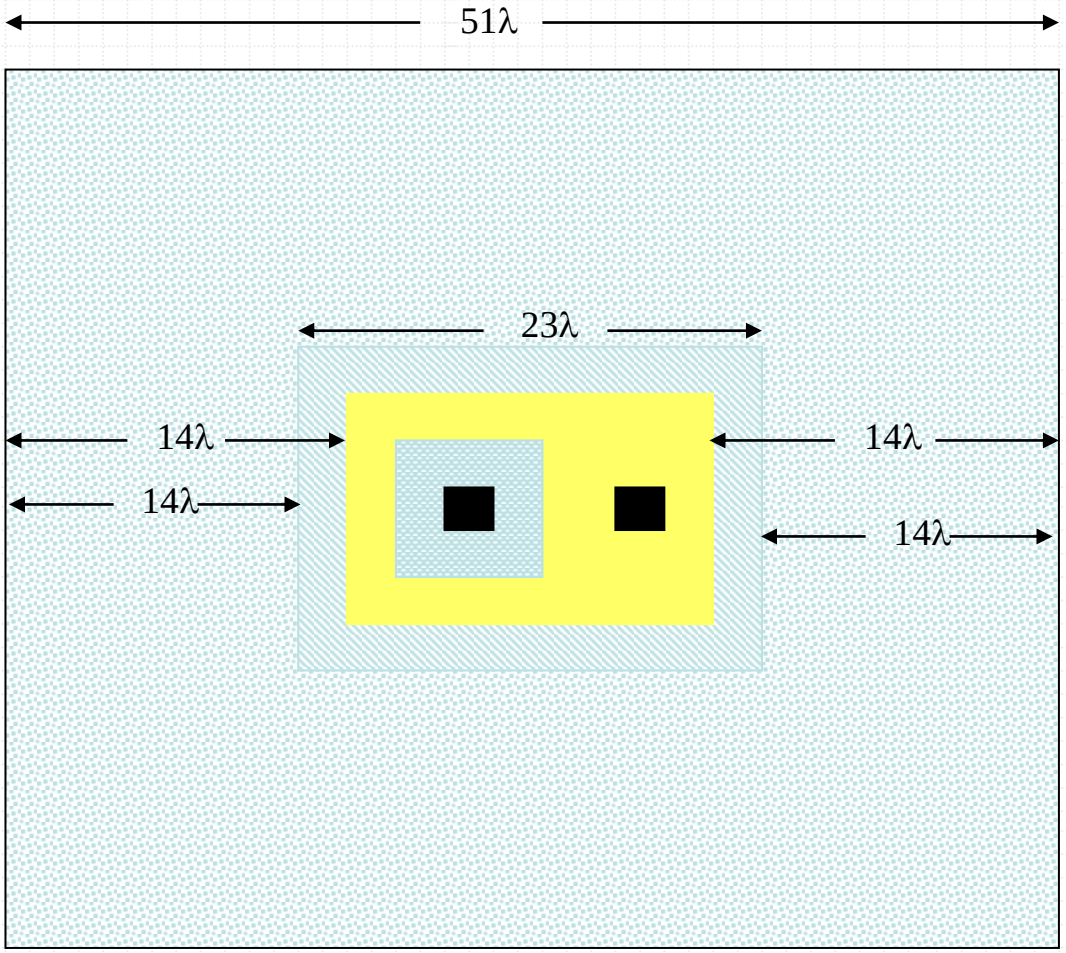
4.5 Spacing to p-base diffusion (for base contact of lateral pnp)	6λ
4.6 Spacing to p-base diffusion (for collector contact of vertical npn)	6λ

Add n-epi region
from design rules 2.3 and 3.3



5. Contact (Black, Mask #5)	
5.1 Size (exactly)	$4\lambda \times 4\lambda$
5.2 Spacing	2λ
5.3 Metal overlap of contact	λ
5.4 n^+ emitter diffusion overlap of contact	2λ
5.5 p-base diffusion overlap of contact	2λ
5.6 p-base to n^+ emitter	3λ
5.7 Spacing to isolation diffusion	4λ
6. Metalization (Blue, Mask #6)	
6.1 Width	2λ
6.2 Spacing	2λ
6.3 Bonding pad size	$100\ \mu \times 100\ \mu$
6.4 Probe pad size	$75\ \mu \times 75\ \mu$
6.5 Bonding pad separation	$50\ \mu$
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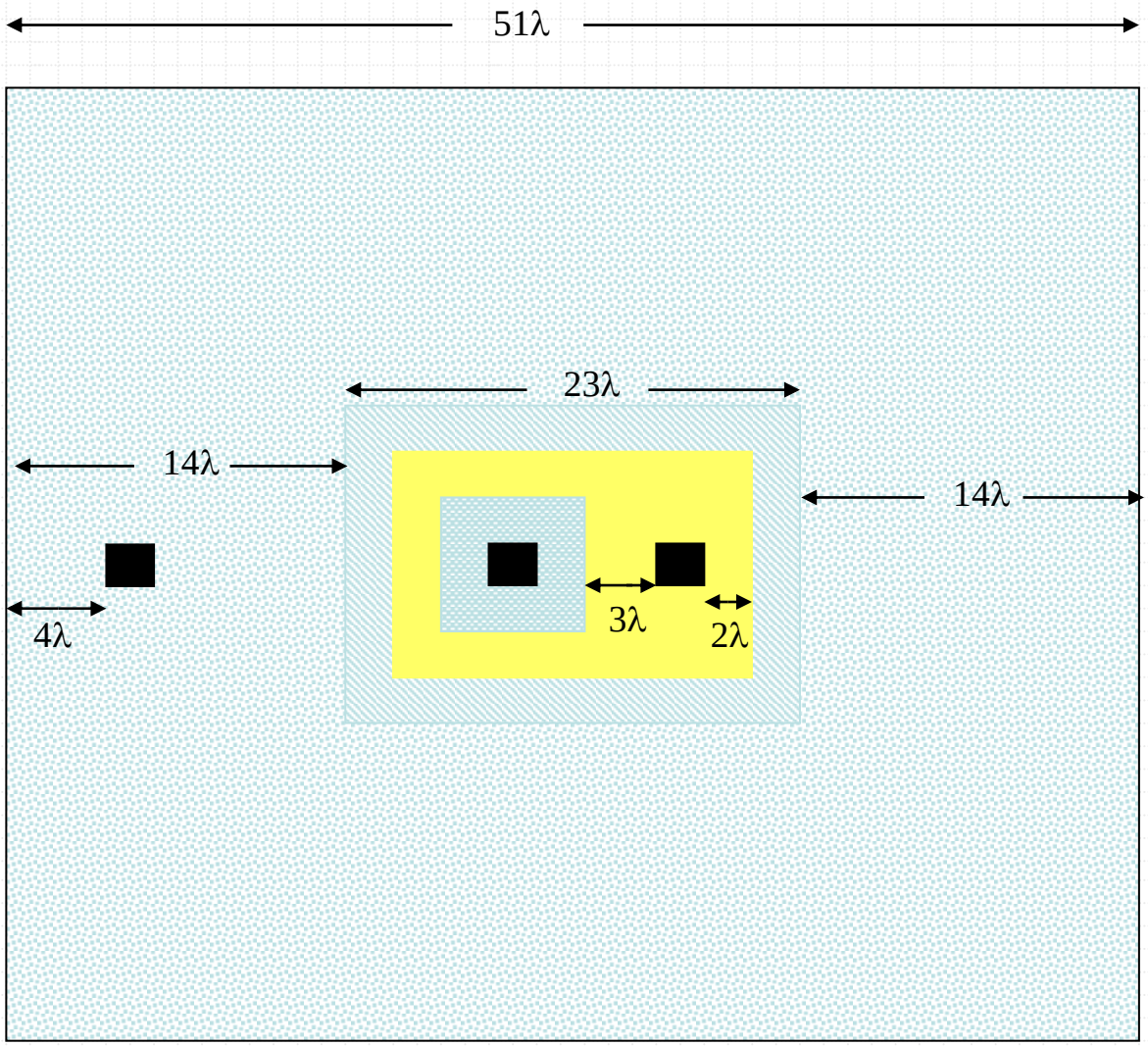
6.8 Pad to circuitry	$40\ \mu$
6.9 Maximum current density	0.8 mA/μ width
7. Passivation (Purple, Mask #7)	
7.1 Minimum bonding pad opening	$90\ \mu \times 90\ \mu$
7.2 Minimum probe pad opening	$65\ \mu \times 65\ \mu$

Add contact to n-epi region from design rules 2.3 and 3.3



Should extend the buried collector to under the collector contact !

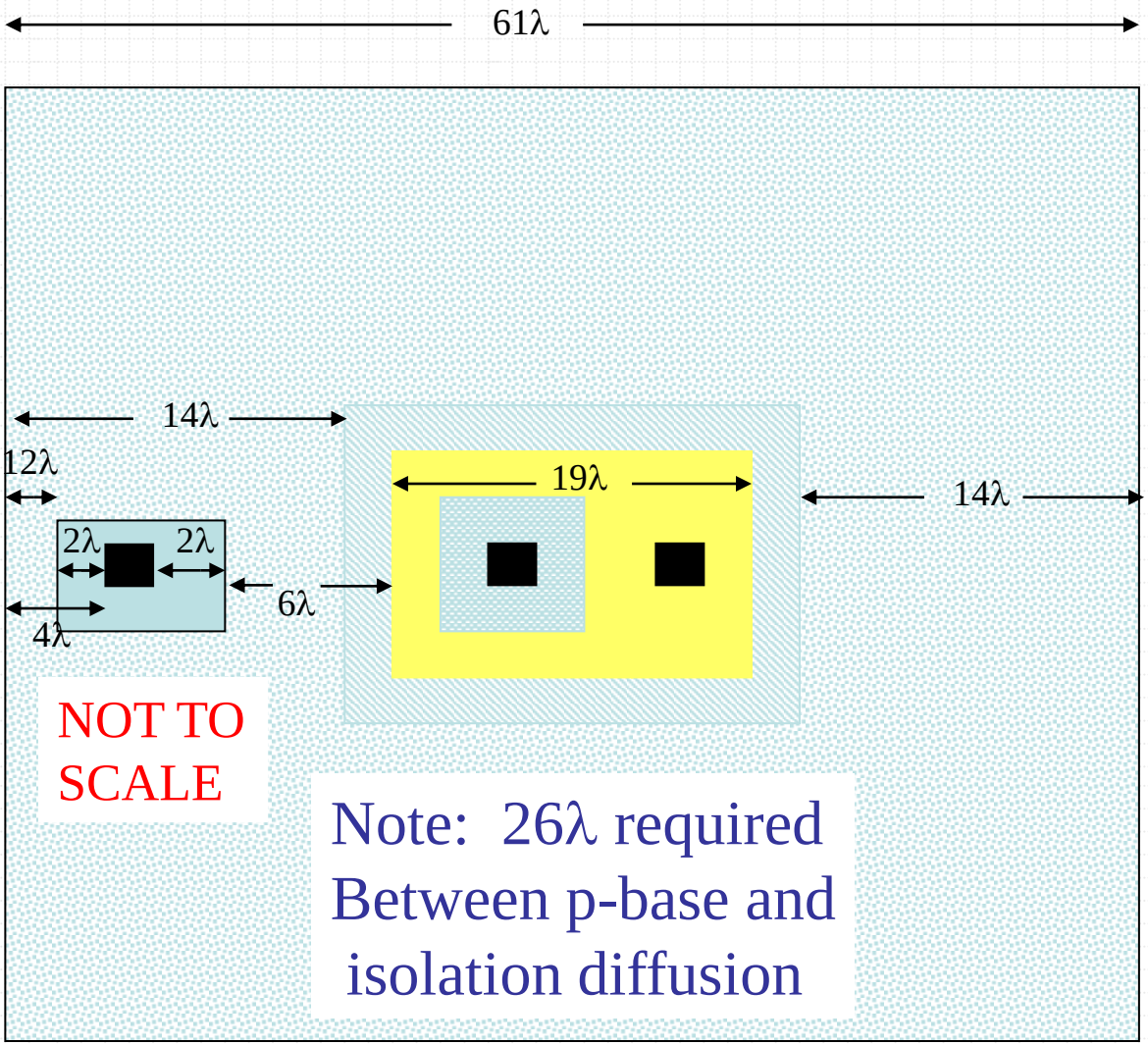
TABLE 2C.2
Design rules for a typical bipolar process ($\lambda = 2.5\ \mu$)
(See Table 2C.3 in color plates for graphical interpretation)

	Dimension
1. n^+ buried collector diffusion (Yellow, Mask #1)	
1.1 Width	3λ
1.2 Overlap of p-base diffusion (for vertical npn)	2λ
1.3 Overlap of n^+ emitter diffusion (for collector contact of vertical npn)	2λ
1.4 Overlap of p-base diffusion (for collector and emitter of lateral pnp)	2λ
1.5 Overlap of n^+ emitter diffusion (for base contact of lateral pnp)	2λ
2. Isolation diffusion (Orange, Mask #2)	
2.1 Width	4λ
2.2 Spacing	24λ
2.3 Distance to n^+ buried collector	14λ
3. p-base diffusion (Brown, Mask #3)	
3.1 Width	3λ
3.2 Spacing	5λ
3.3 Distance to isolation diffusion	14λ
3.4 Width (resistor)	3λ
3.5 Spacing (as resistor)	3λ
4. n^+ emitter diffusion (Green, Mask #4)	
4.1 Width	3λ
4.2 Spacing	3λ
4.3 p-base diffusion overlap of n^+ emitter diffusion (emitter in base)	2λ
4.4 Spacing to isolation diffusion (for collector contact)	12λ
4.5 Spacing to p-base diffusion (for base contact of lateral pnp)	6λ
4.6 Spacing to p-base diffusion (for collector contact of vertical npn)	6λ

5.	Contact (Black, Mask #5)	
	5.1 Size (exactly)	$4\lambda \times 4\lambda$
	5.2 Spacing	2λ
	5.3 Metal overlap of contact	λ
	5.4 n^+ emitter diffusion overlap of contact	2λ
	5.5 p-base diffusion overlap of contact	2λ
	5.6 p-base to n^+ emitter	3λ
	5.7 Spacing to isolation diffusion	4λ
6.	Metalization (Blue, Mask #6)	
	6.1 Width	2λ
	6.2 Spacing	2λ
	6.3 Bonding pad size	$100\ \mu \times 100\ \mu$
	6.4 Probe pad size	$75\ \mu \times 75\ \mu$
	6.5 Bonding pad separation	$50\ \mu$
	6.6 Bonding to probe pad	$30\ \mu$
	6.7 Probe pad separation	$30\ \mu$
	6.8 Pad to circuitry	$40\ \mu$
	6.9 Maximum current density	0.8 mA/μ width
7.	Passivation (Purple, Mask #7)	
	7.1 Minimum bonding pad opening	$90\ \mu \times 90\ \mu$
	7.2 Minimum probe pad opening	$65\ \mu \times 65\ \mu$

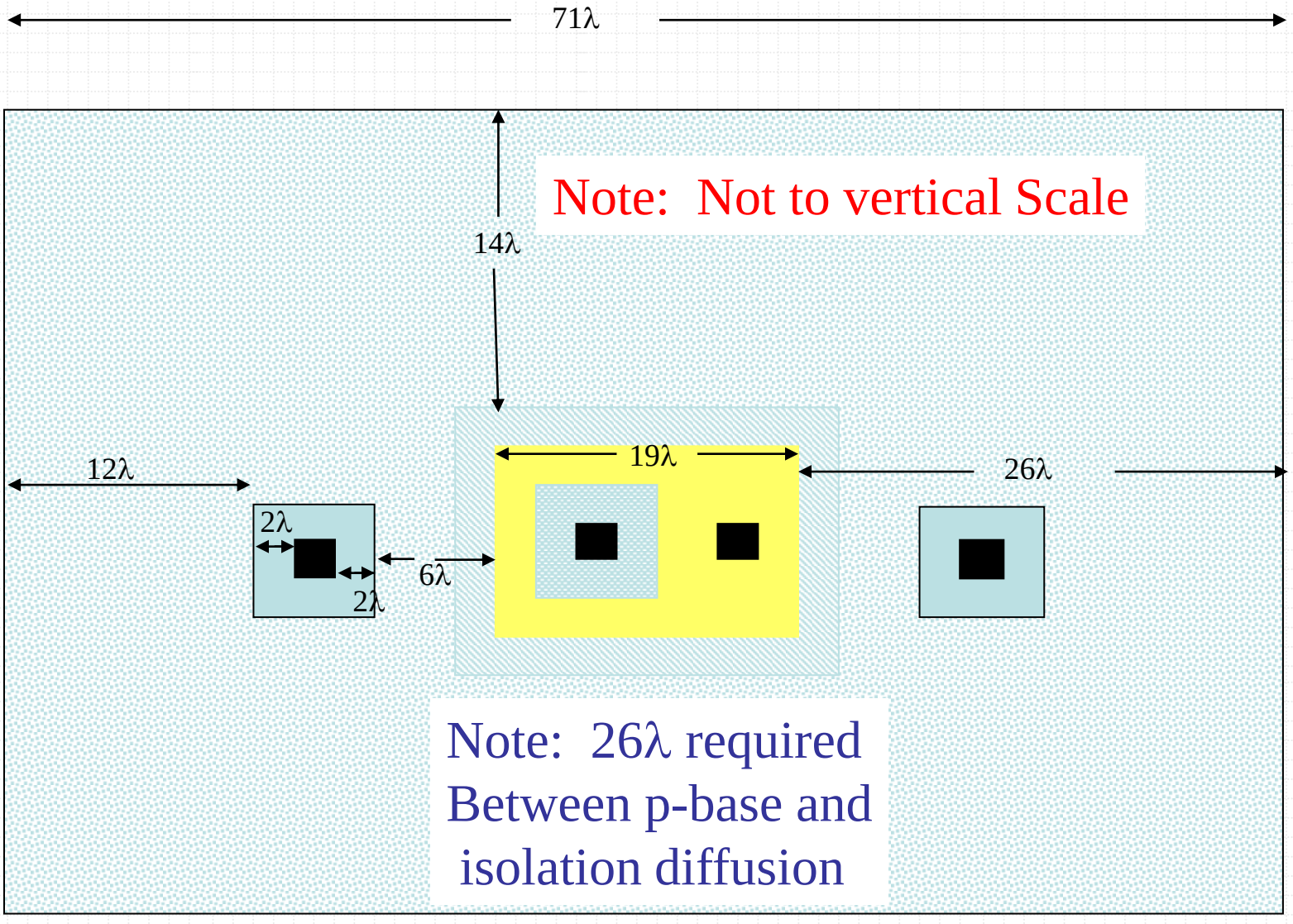
But, there are some rather strict rules relating to the epi contact

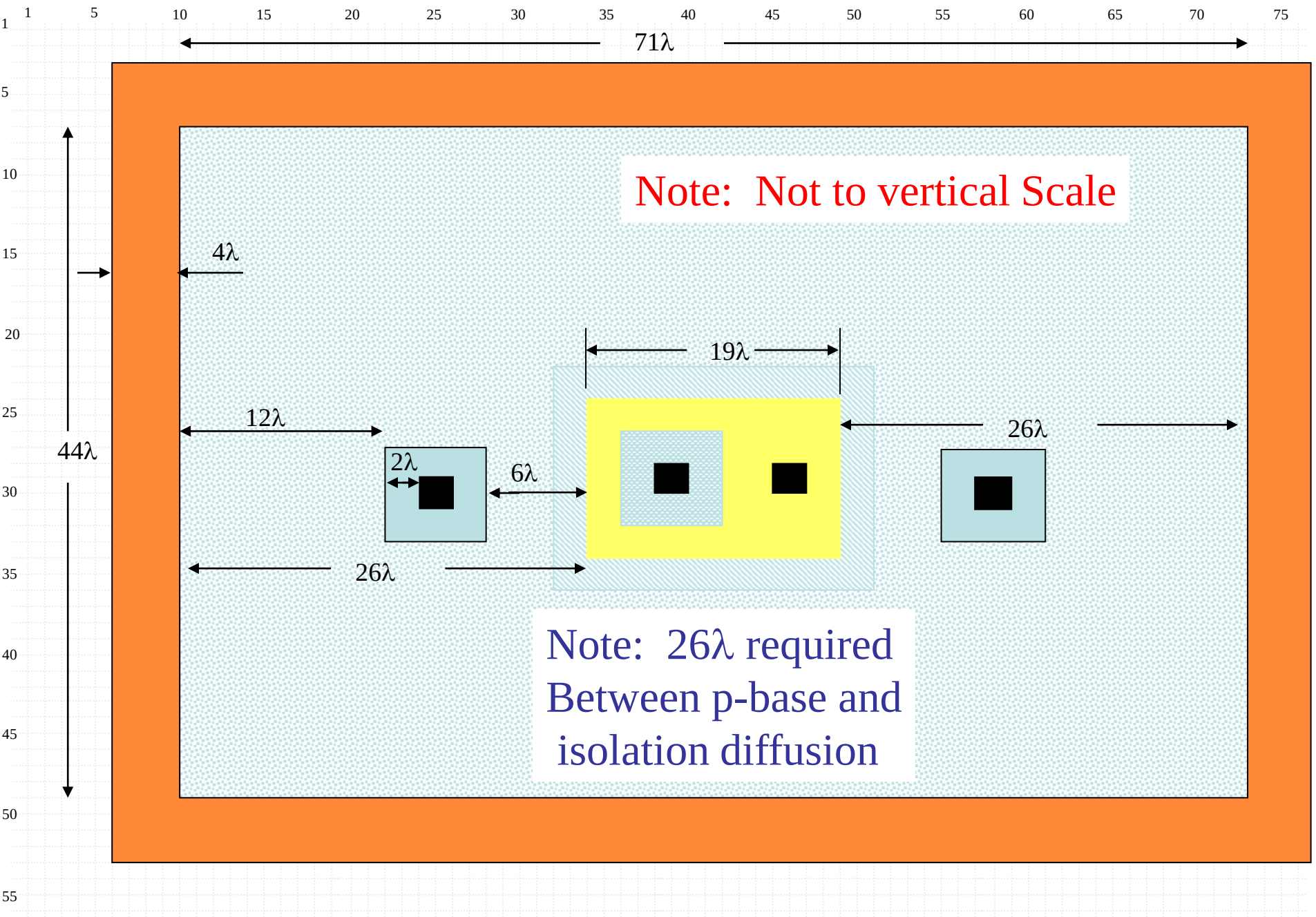
from (left to right) rules 4.4, 5.4, 4.6



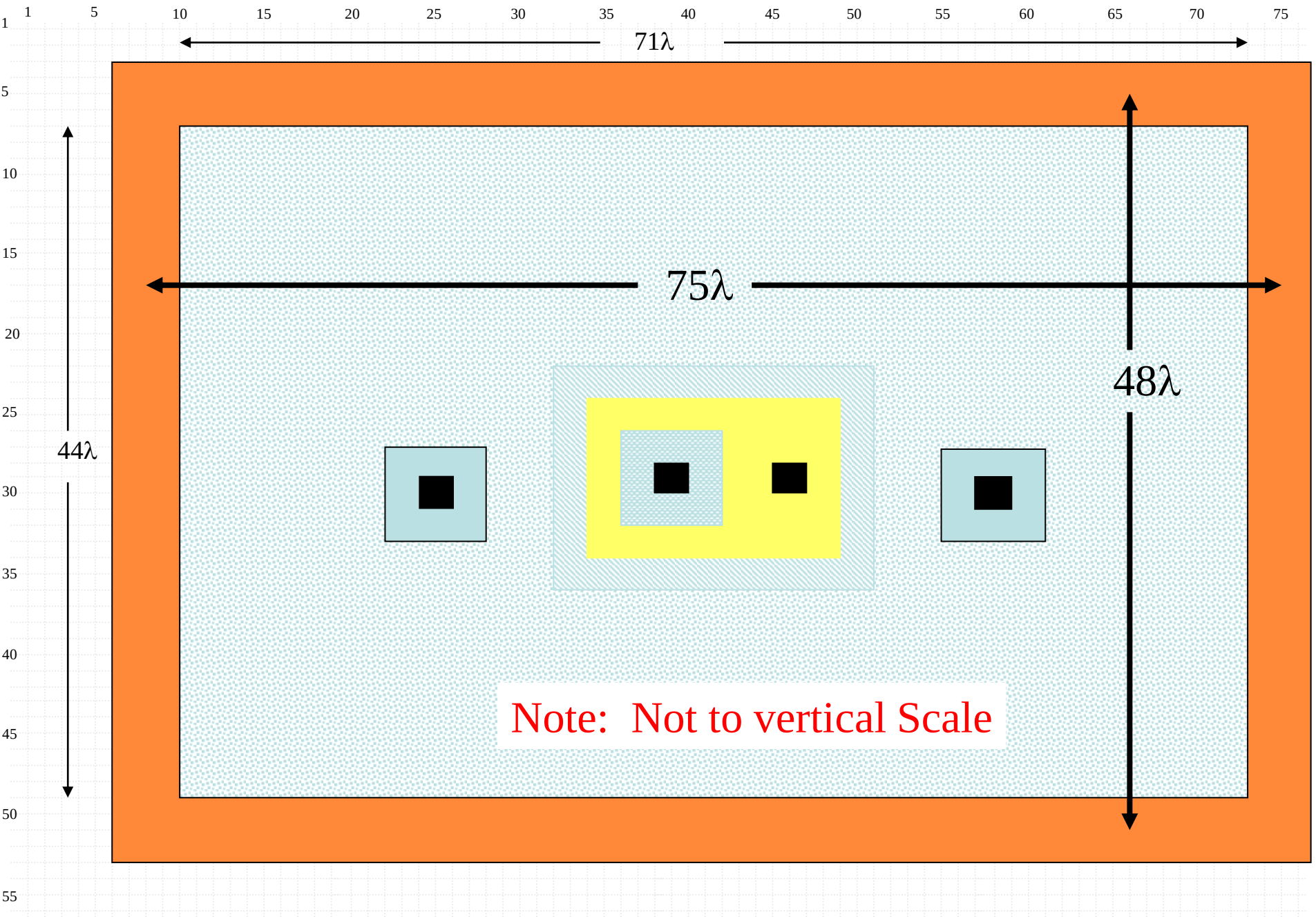
Should extend the buried collector to under the collector contact !

Consider a structure with a collector contact on both sides of epi

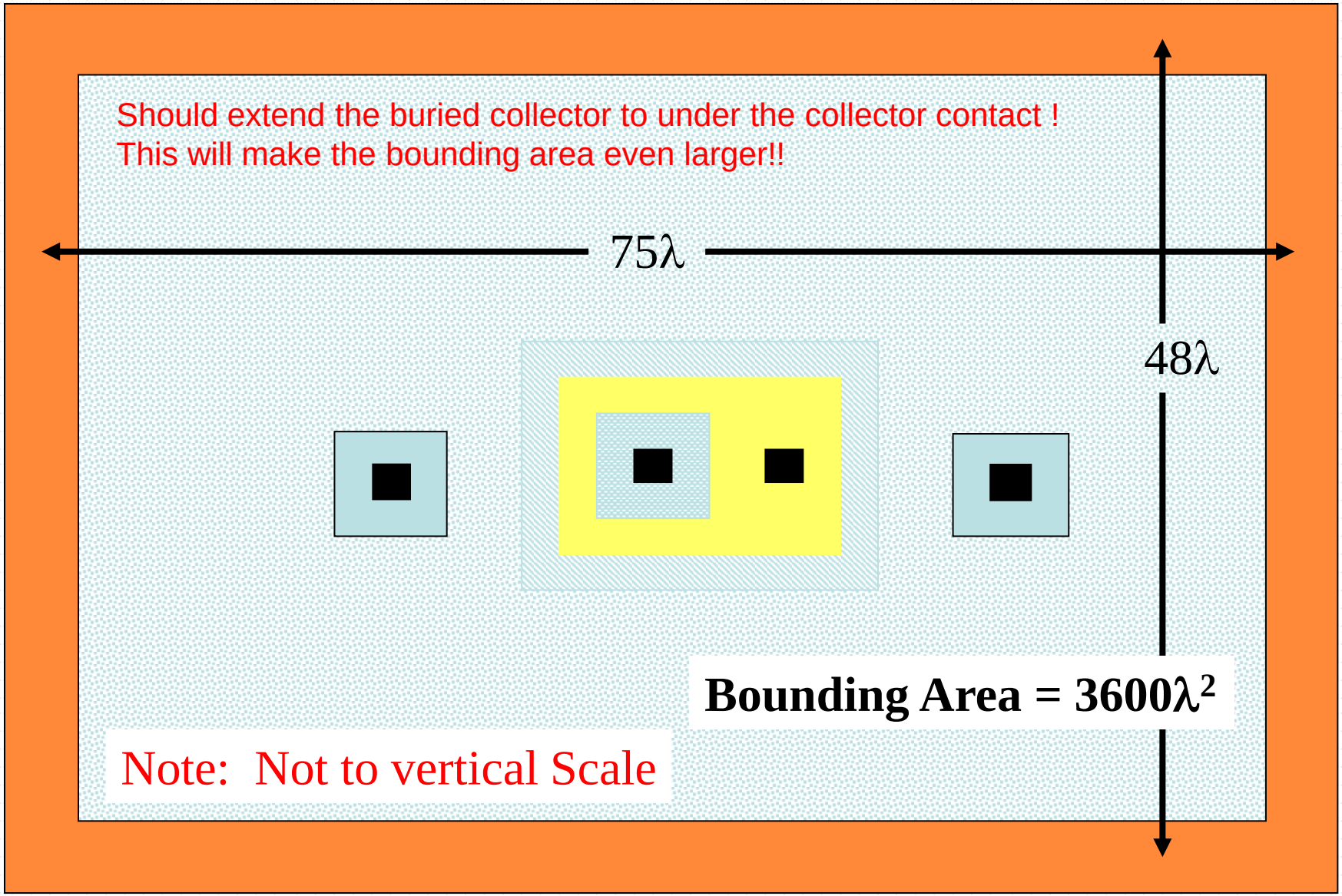




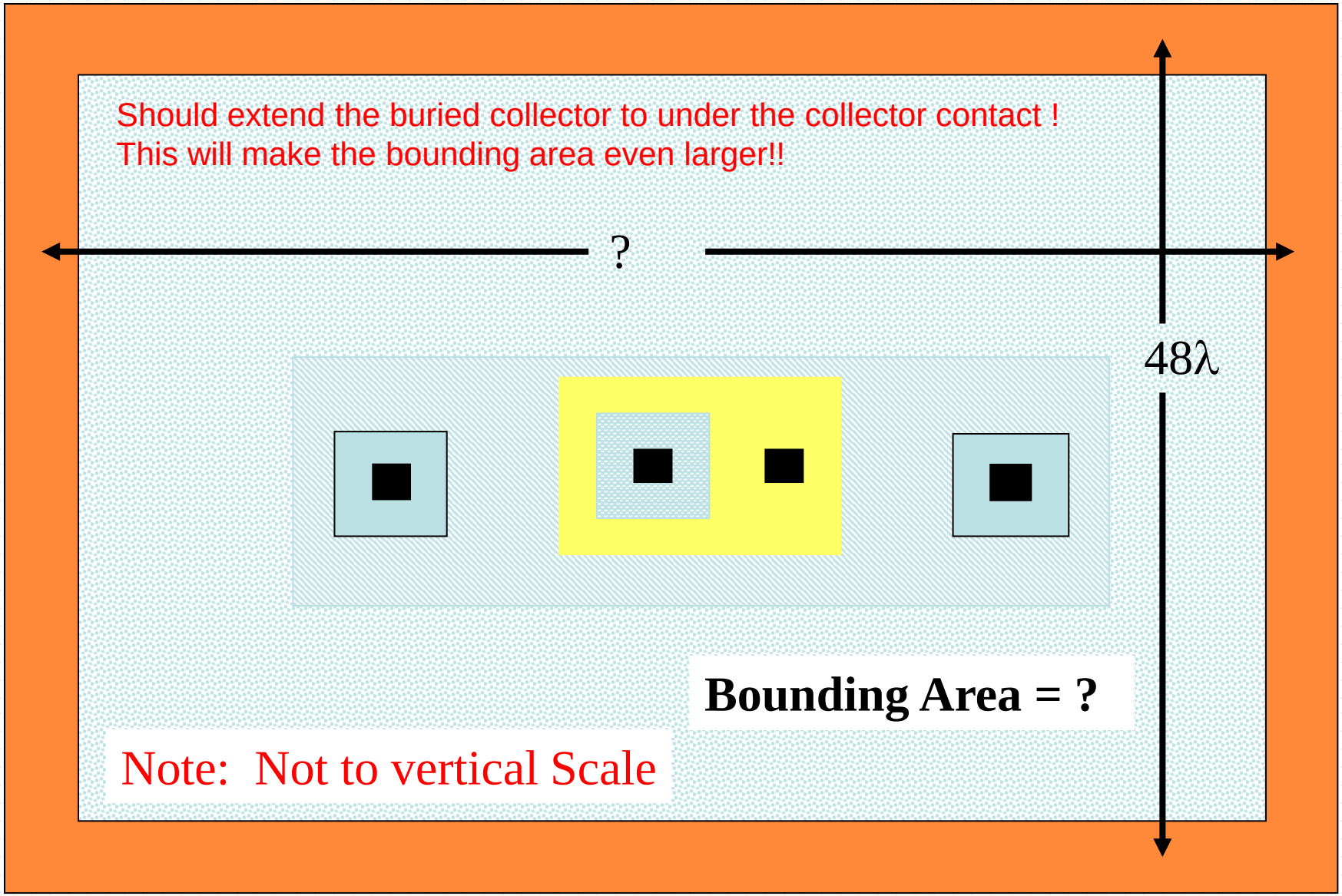
Should extend the buried collector to under the collector contact !



Should extend the buried collector to under the collector contact !

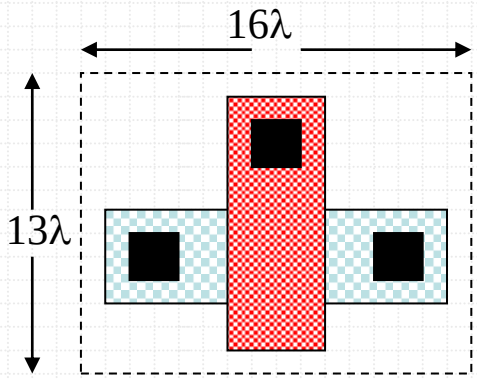


Major contributor to large size of BJT is the isolation diffusion which diffuses laterally a large distance beyond the drawn edges of the isolation mask



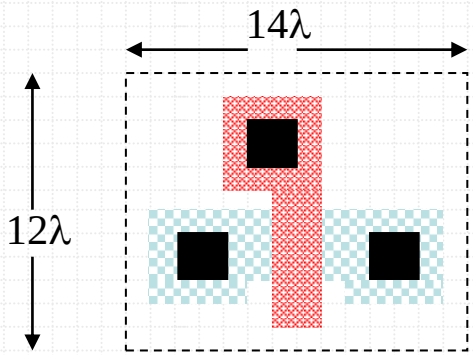
Major contributor to large size of BJT is the isolation diffusion which diffuses laterally a large distance beyond the drawn edges of the isolation mask

Comparison with Area for n-channel MOSFET in Bulk CMOS



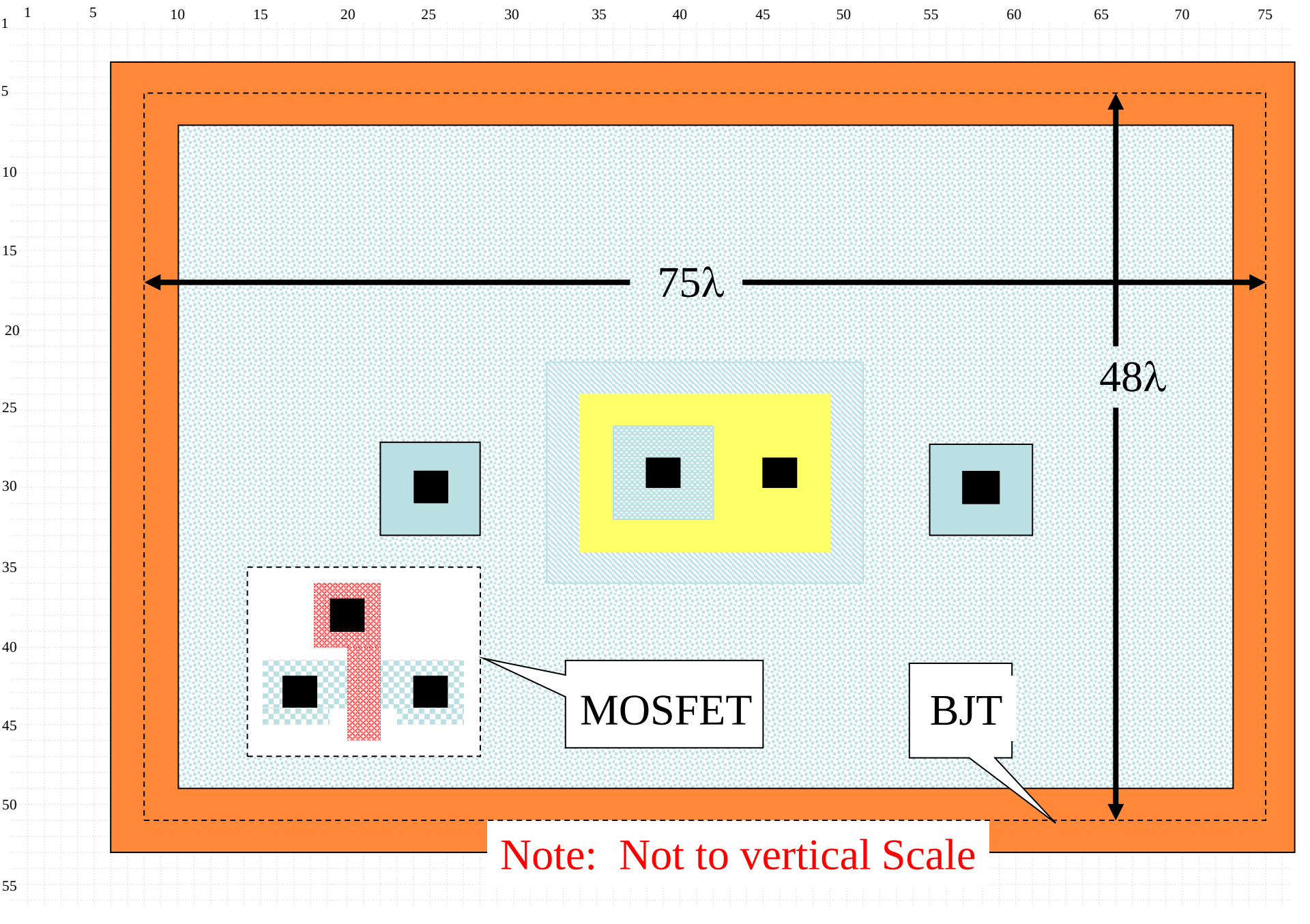
Bounding Area = $208\lambda^2$

Minimum-Sized MOSFET



Bounding Area = $168\lambda^2$

Active Area = $6\lambda^2$


75λ
48λ
MOSFET
BJT
Note: Not to vertical Scale

Area Comparison between BJT and MOSFET

- BJT Area = 3600 λ^2
- n-channel MOSFET Area = 168 λ^2
- Area Ratio = 21:1

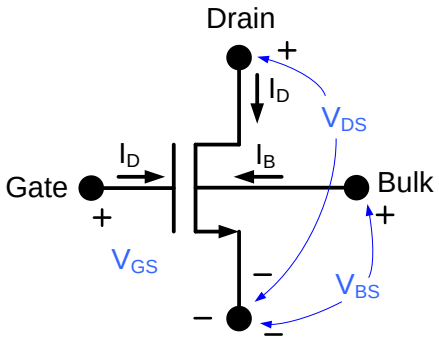
Small-Signal Models

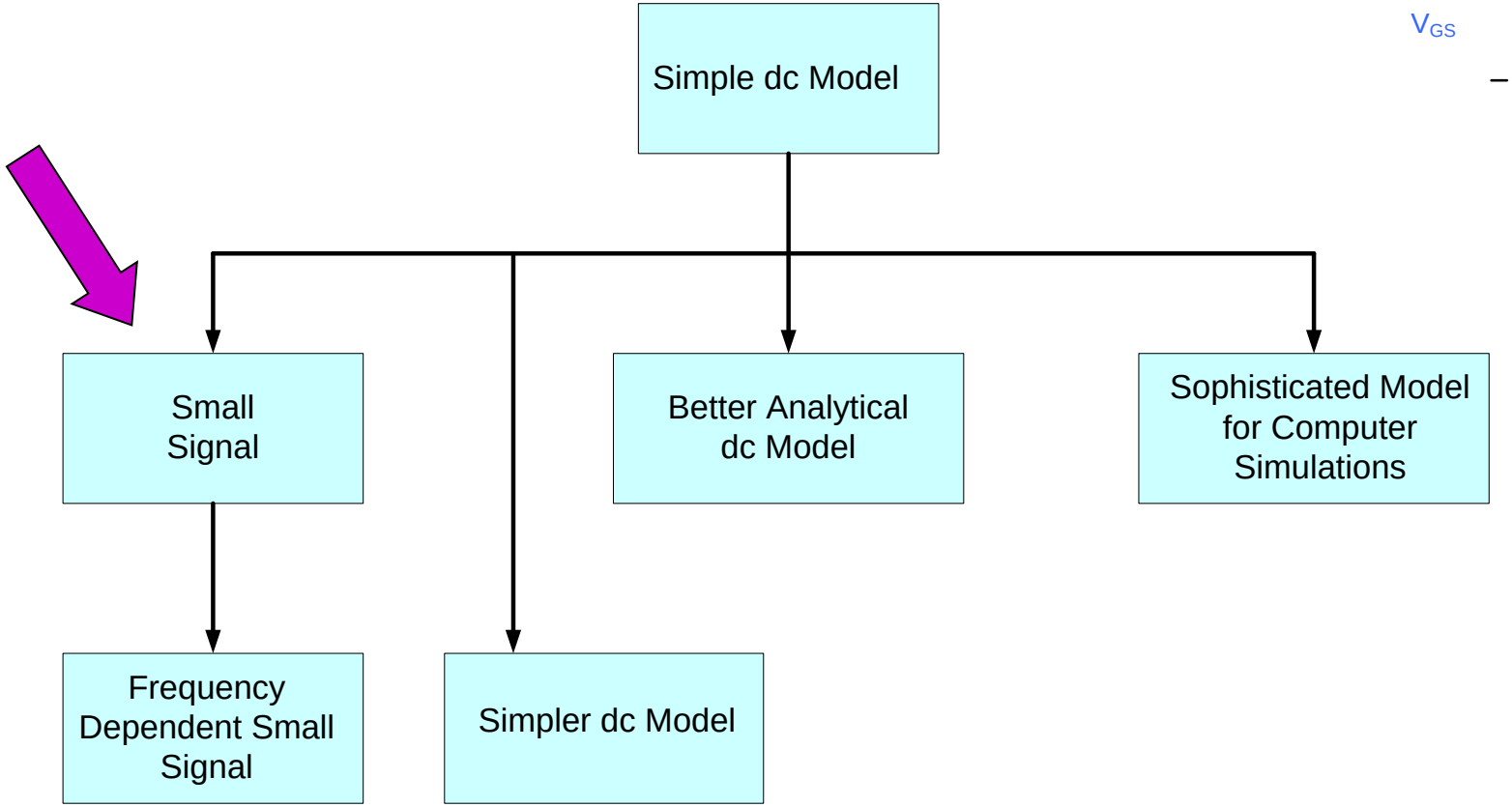
- MOSFET
- BJT
- Diode (of limited use)

Modeling of the MOSFET

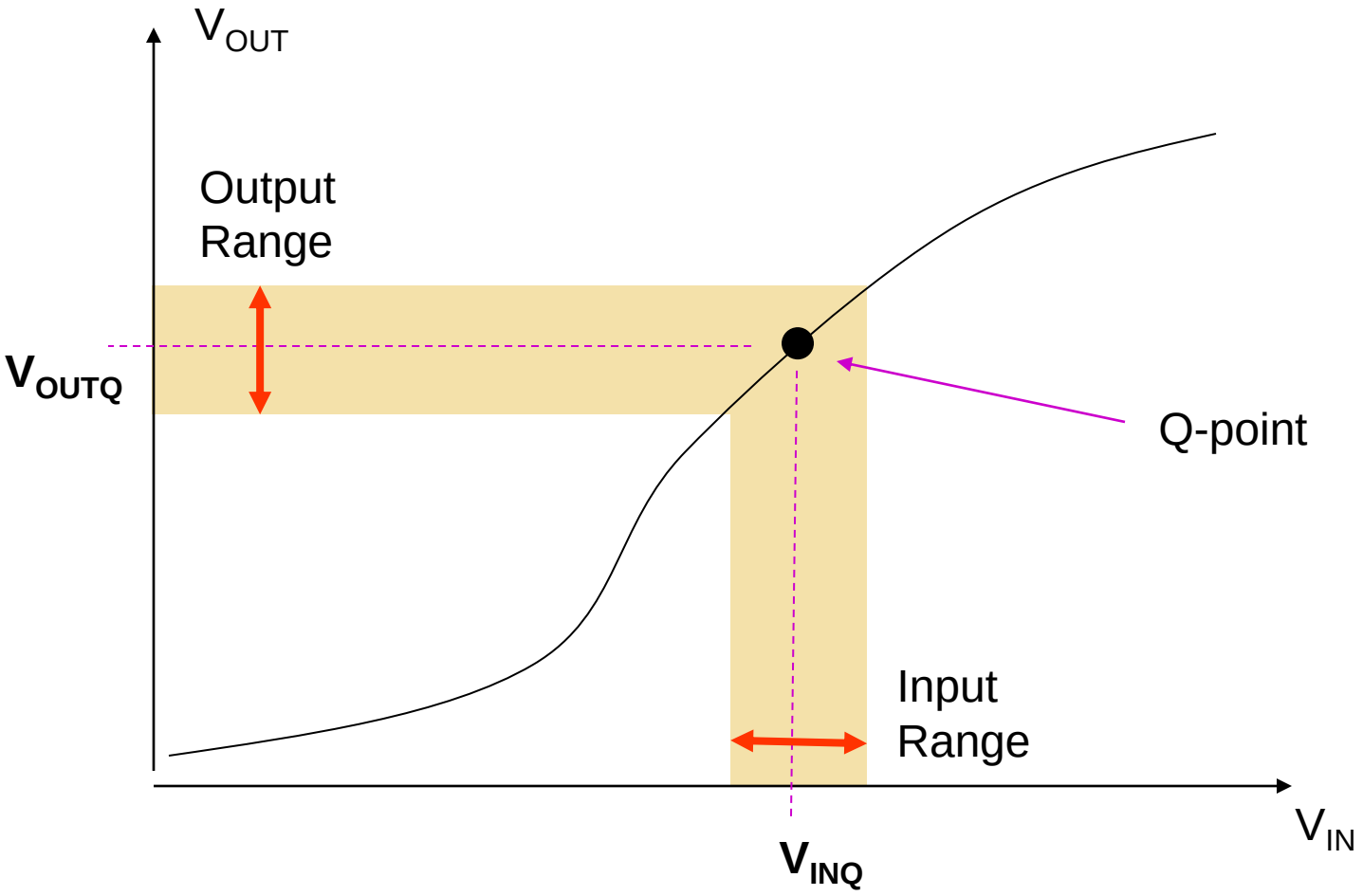
Goal: Obtain a mathematical relationship between the port variables of a device.

$$I_D = f_1(V_{GS}, V_{DS}, V_{BS})$$
$$I_G = f_2(V_{GS}, V_{DS}, V_{BS})$$
$$I_B = f_3(V_{GS}, V_{DS}, V_{BS})$$



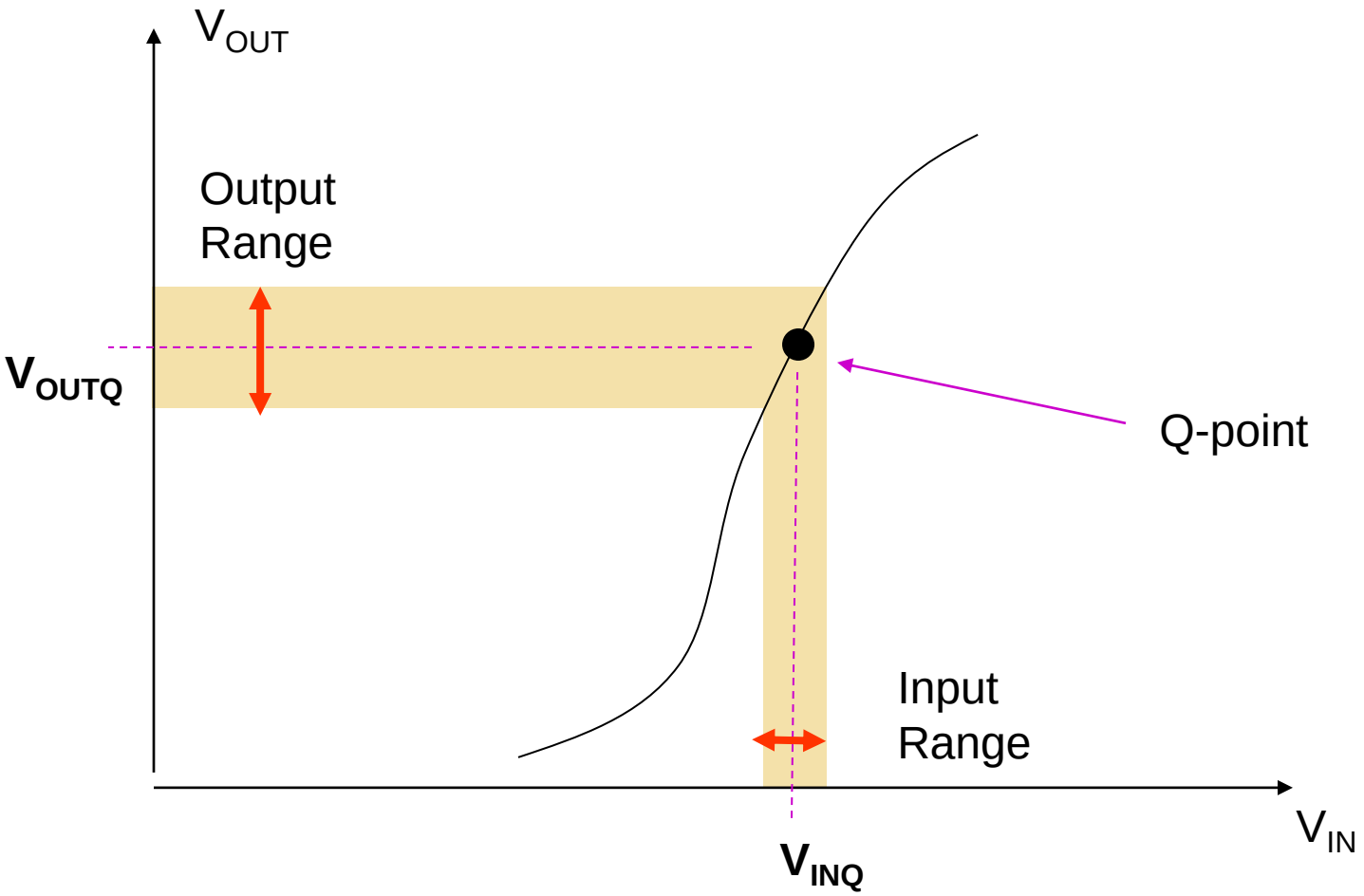


Small-Signal Operation



Throughout the small input range, the “distant” nonlinearities do not affect performance

Small-Signal Operation

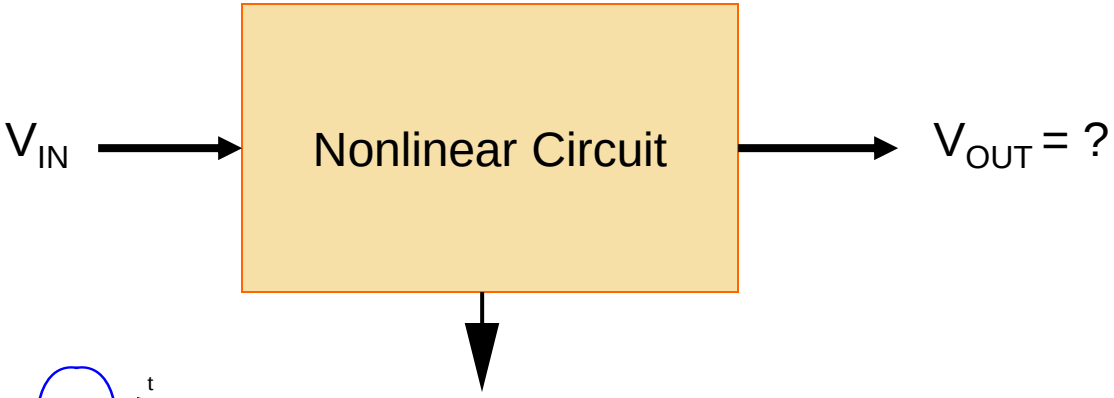


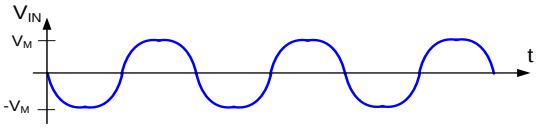
- If slope is steep, output range can be much larger than input range
- The slope can be viewed as the voltage gain of the circuit
- Nonlinear circuit behaves as a linear circuit near Q-point with small-signal inputs

Small signal operation of nonlinear circuits

$V_{IN}=V_m \sin\omega t + V_{INQ}$

V_M is small





- **Small signal concepts often apply when building amplifiers**
- **If small signal concepts do not apply, usually the amplifier will not perform well**
- **Small signal operation is usually synonymous with “locally linear”**
- **Small signal operation is relative to an “operating point”**

Operating Point of Electronic Circuits

Often interested in circuits where a small signal input is to be amplified (e.g. V_M in previous slide is small)

The electrical port variables where the small signals goes to 0 are termed the Operating Points, the Bias Points, the Quiescent Points, or simply the Q-Points

By setting the small signal inputs to 0, it means replacing small voltage inputs with short circuits and small current inputs with open circuits

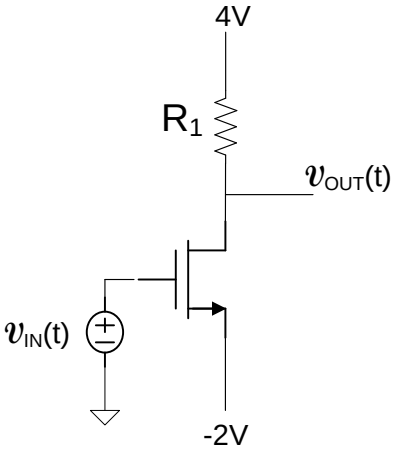
When analyzing small-signal amplifiers, it is necessary to obtain the Q-point

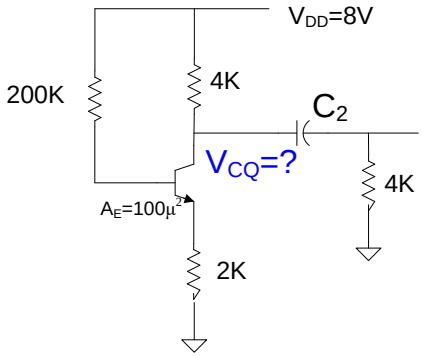
When designing small-signal amplifiers, establishing of the desired Q-point is termed "biasing"

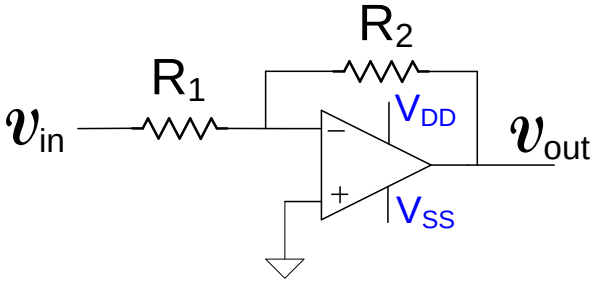
- Capacitors become open circuits (and inductors short circuits) when determining Q-points
- Simplified dc models of the MOSFET (saturation region) or BJT (forward active region) are usually adequate for determining the Q-point in practical amplifier circuits
- DC voltage and current sources remain when determining Q-points
- Small-signal voltage and current sources are set to 0 when determining Q-points

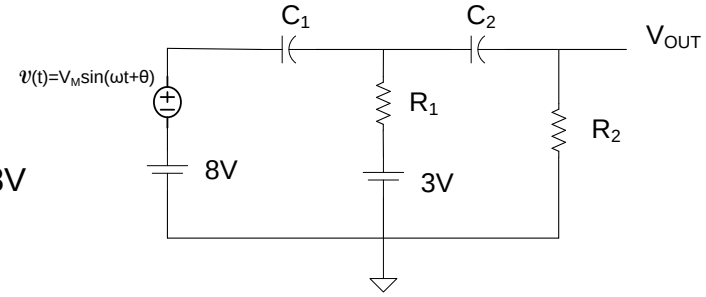
Operating Point of Electronic Circuits

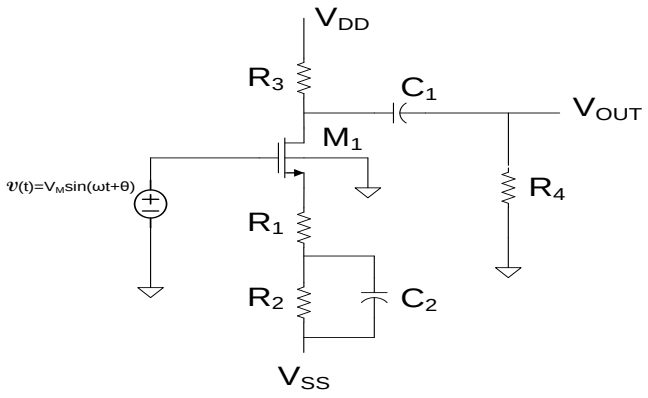
(small signal inputs, if there are any, are set to 0)

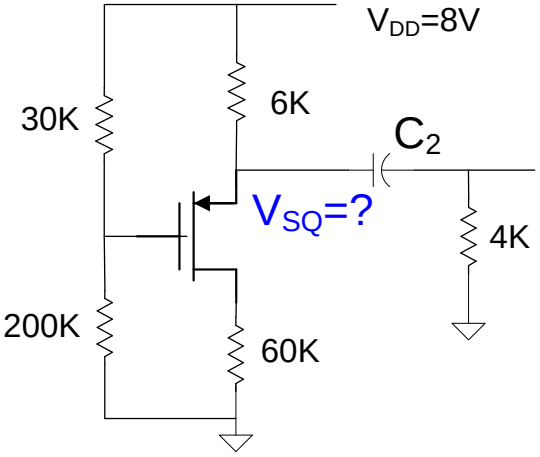








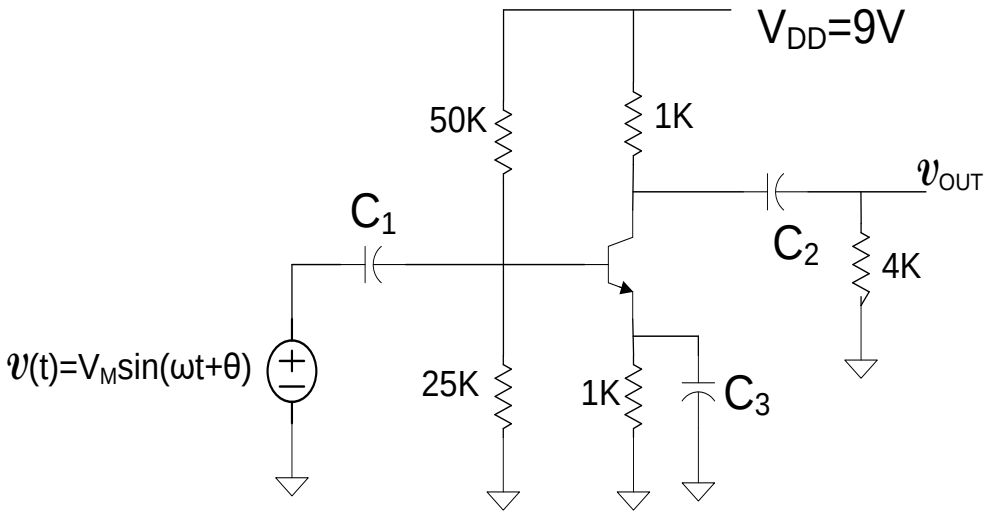




Operating Point Analysis of MOS and Bipolar Devices

Example:

Determine V_{OUTQ} and V_{CQ}

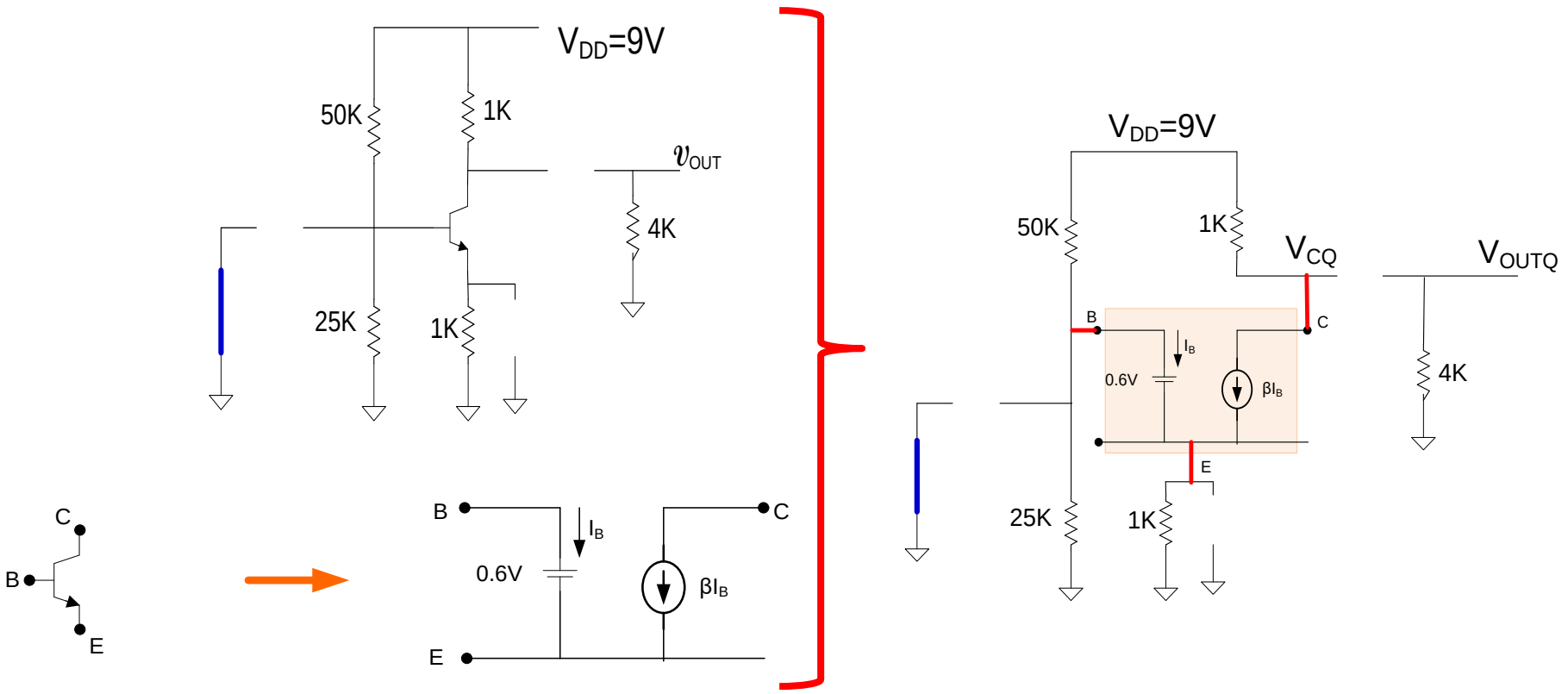


Will formally go through the process in this example, will go into more detail about finding the operating point later

Operating Point Analysis of MOS and Bipolar Devices

Example:

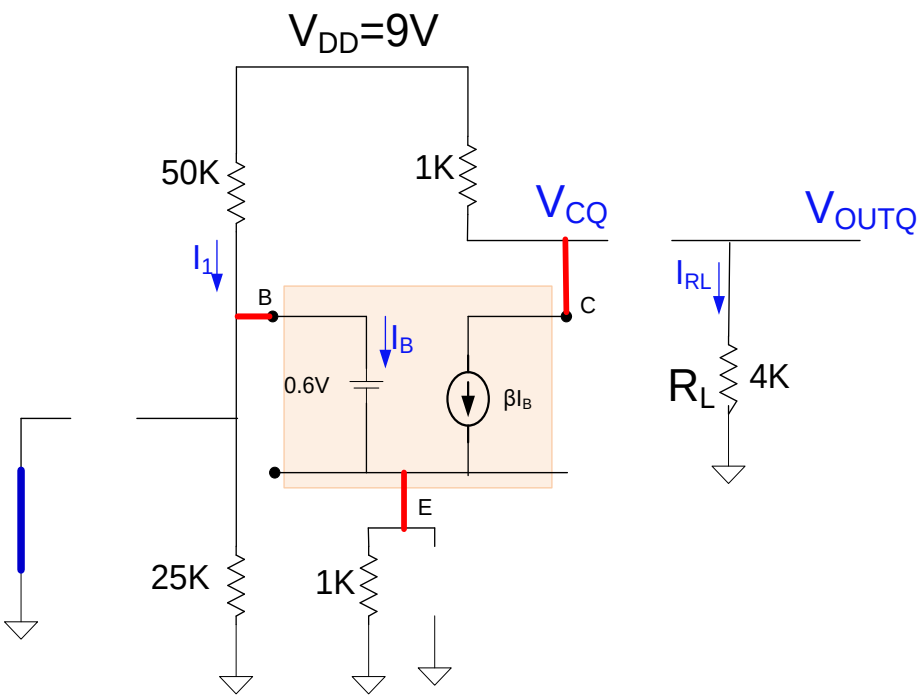
Determine V_{OUTQ} and V_{CQ}



Operating Point Analysis of MOS and Bipolar Devices

Example:

Determine V_{OUTQ} and V_{CQ}



Assume β=100

Assume $I_B << I_1$ (must verify)

$$V_{BQ} = \frac{9V}{3} = 3V$$

$$V_{EQ} = 3V - 0.6V = 2.4V$$

$$I_{EQ} = I_{CQ} = \frac{2.4V}{1K} = 2.4mA$$

$$V_{CQ} = 9V - I_{CQ} \bullet 1K = 9V - 2.4V = 6.6V$$

$V_{OUTQ} = I_{RL} \bullet 4K = 0V$

V_{CQ}=6.6V

V_{OUTQ}=0V

Amplification with Transistors

From Wikipedia: (Oct. 2019 and October 2020)

> An **amplifier**, **electronic amplifier** or (informally) **amp** is an electronic device that can increase the power of a signal (a time-varying voltage or current).

What is the “power” of a signal?

Can an amplifier make decisions?

Does Wikipedia have such a basic concept right?

Amplification with Transistors

From Wikipedia: (Oct. 2019, Oct. 2020, Oct 2021)

An **amplifier**, **electronic amplifier** or (informally) **amp** is an electronic device that can increase the power of a signal (a time-varying voltage or current).

It is a two-port electronic circuit that uses electric power from a power supply to increase the amplitude of a signal applied to its input terminals, producing a proportionally greater amplitude signal at its output. The amount of amplification provided by an amplifier is measured by its gain: the ratio of output voltage, current, or power to input. An amplifier is a circuit that has a power gain greater than one.[1][2][3]

Self-inconsistent definition !

Amplification with Transistors

From Wikipedia: (Feb. 2017)

An **amplifier**, **electronic amplifier** or (informally) **amp** is an electronic device that increases the power of a signal (a time varying voltage or current.

From Wikipedia: (Oct. 2015)

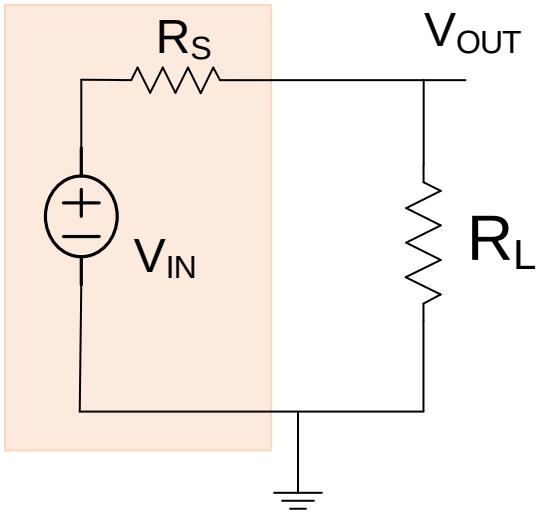
An **amplifier**, **electronic amplifier** or (informally) **amp** is an electronic device that increases the power of a signal.

From Wikipedia: (approx. 2010)

Generally, an **amplifier** or simply **amp**, is any device that changes, usually increases, the amplitude of a signal. The "signal" is usually voltage or current.

These “minor” differences in definition are not trivial !

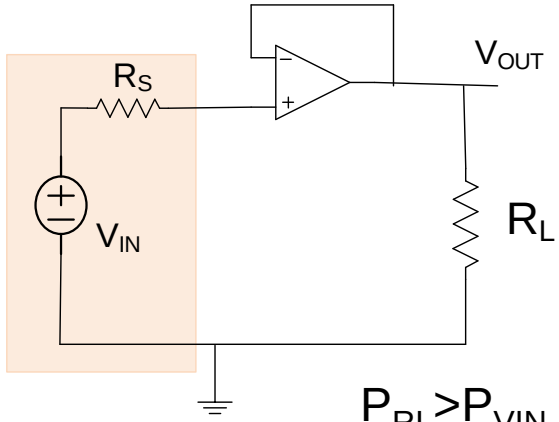
Signal and Power Levels



$P_{RL}<P_{VIN}$

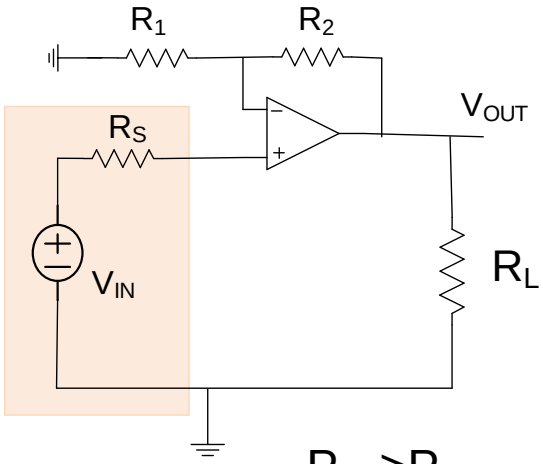
$V_{OUT}<V_{IN}$

P_{RL} will be maximum when load impedance matches source impedance



$P_{RL}>P_{VIN}$

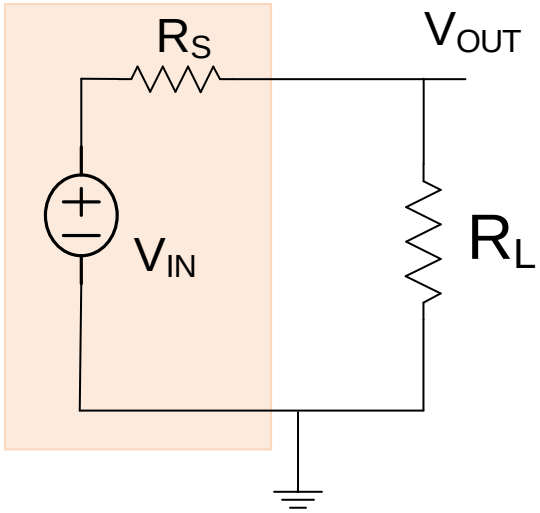
$V_{OUT}=V_{IN}$



$P_{RL}>P_{VIN}$

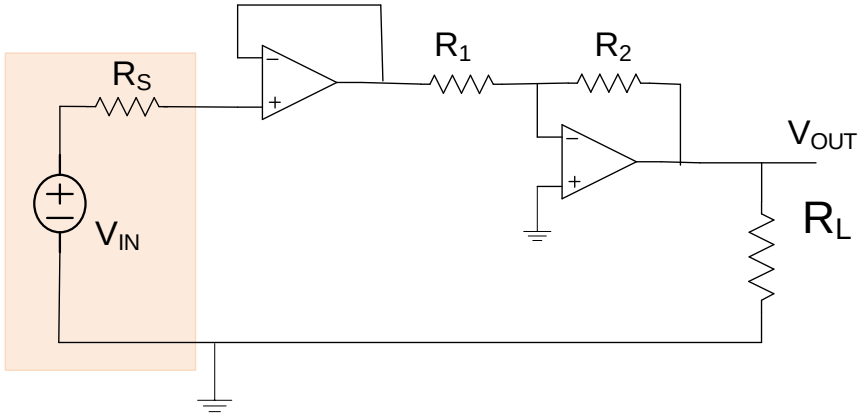
V_{OUT} can be larger of smaller than V_{IN}

Signal and Power Levels



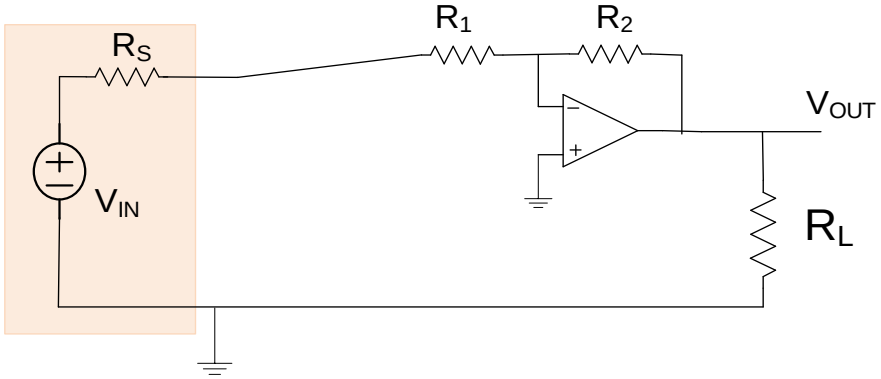
$P_{RL}<P_{VIN}$

$V_{OUT}<V_{IN}$



$P_{RL}>P_{VIN}$

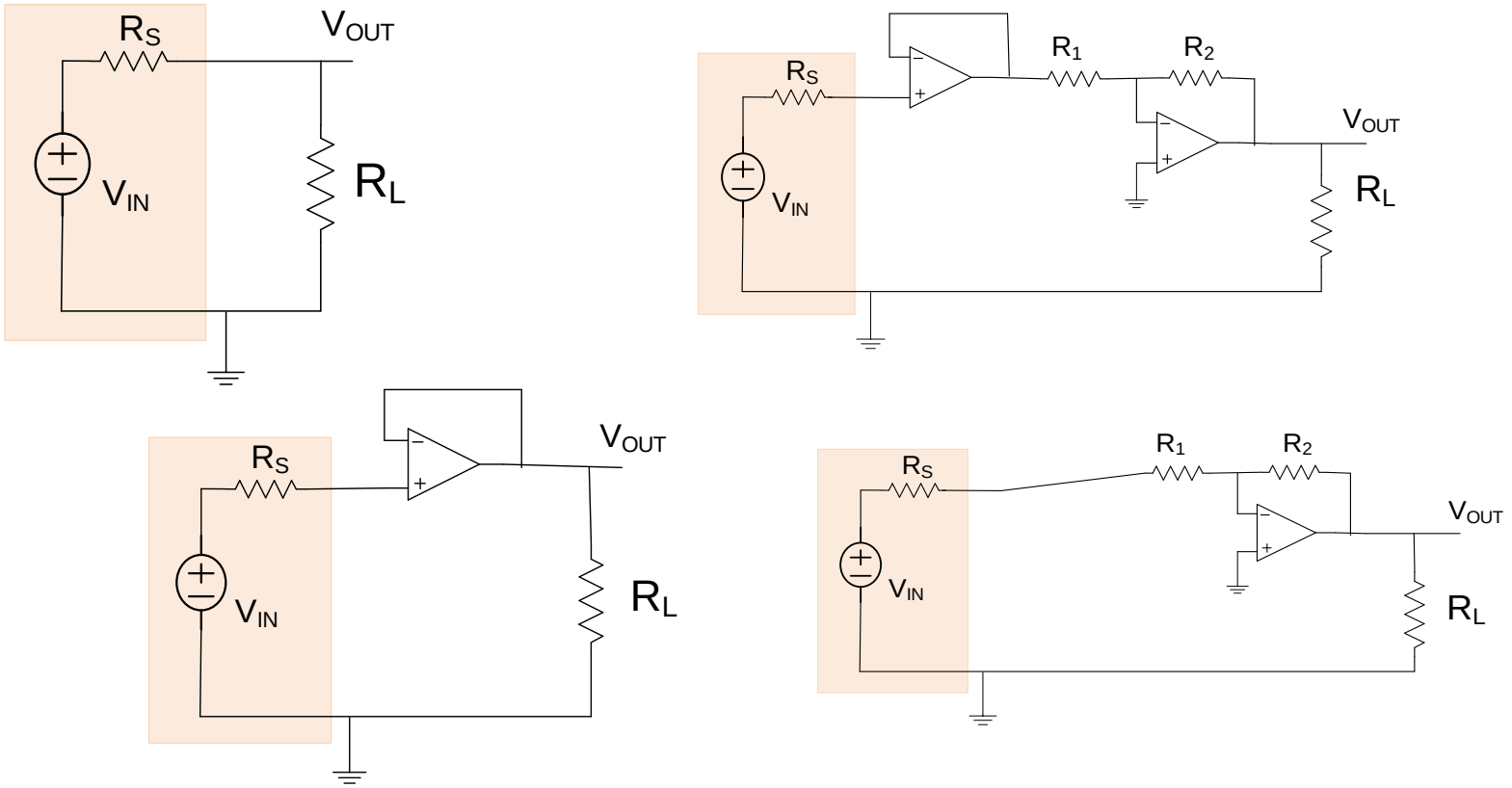
V_{OUT} can be larger or smaller than V_{IN}



V_{OUT} can be larger of smaller than V_{IN}

P_{RL} can be larger of smaller than P_{VIN}

Signal and Power Levels



In most electronic circuit “amplifier” applications, there is little concern about whether the power in the load is larger or smaller than the power supplied by the source

Impedance matching for the purpose of delivering power to a load is seldom of concern or even used in most electronic circuits

Amplification with Transistors

From Wikipedia: (Oct. 2019 , March 2020, Oct 2021)

An **amplifier**, **electronic amplifier** or (informally) **amp** is an electronic device that can increase the power of a signal (a time-varying voltage or current).

- It is difficult to increase the voltage or current very much with passive RC circuits
- Voltage and current levels can be increased a lot with transformers but transformers not practical in integrated circuits
- Power levels can not be increased with passive elements (R, L, C, and Transformers)

- Often an amplifier is defined to be a circuit that **can** be used to increase power delivered to a resistive load (be careful with Wikipedia and WWW even when some of the most basic concepts are discussed)
- Transistors can be used to increase not only signal levels but power levels to a load
- In transistor circuits, power that is delivered in the signal path is supplied by a biasing network
- Signals that are amplified are often not time varying

In the electronic community, there is often little or no concern about the power delivered to a load and the term “amplifier” generally refers to a device that changes the level of a voltage or current or converts from one unit to another (V to I or I to V)

Amplification with Transistors

From Wikipedia: (Oct. 2019 and March 2020)

An **amplifier**, **electronic amplifier** or (informally) **amp** is an electronic device that can increase the power of a signal (a time-varying voltage or current).

From Wikipedia: (Oct. 2015)

It does this by taking energy from a power supply and controlling the output to match the input signal shape but with a larger amplitude. In this sense, an amplifier modulates the output of the power supply to make the output signal stronger than the input signal.

Stay Safe and Stay Healthy !

End of Lecture 22